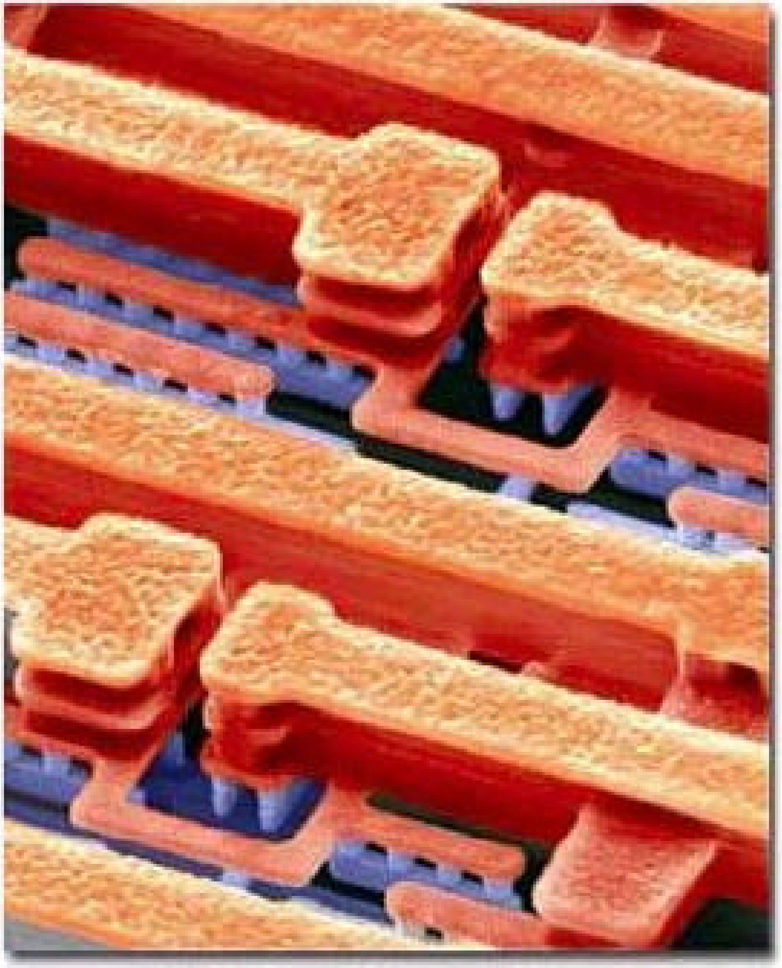
Impact of Mechanics on Reliability for Interconnect Structures in Microelectronics

Paul S. Ho
Microelectronics Research Center
University of Texas at Austin

UT Seminar 04_2006

- Technological needs for low k dielectrics
- Chemical bond and polarizability
- Mechanics of Dielectric Cracking & Interface Delamination
- Chip package interaction
- Summary

Interconnect Wiring System



SEN view of Copper Interconnect
(IBM Microelectronics)

- Interconnect functions as a wiring system to distribute
  - Clock signals
  - Electrical signals
  - Power distribution
  - Ground distributions

  among circuits on a chip (intrachip interconnects) or among chips (interchip interconnects)
- Interconnect system has to be optimized for speed, density, signal noise, power distribution, cost and yield

High-Performance Multi-chip Module for IBM 3080 Computer System

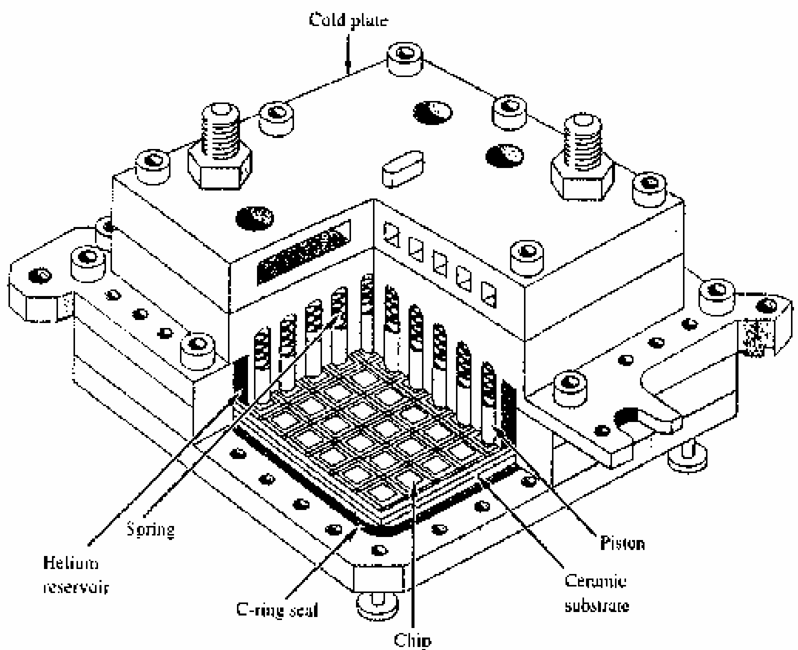
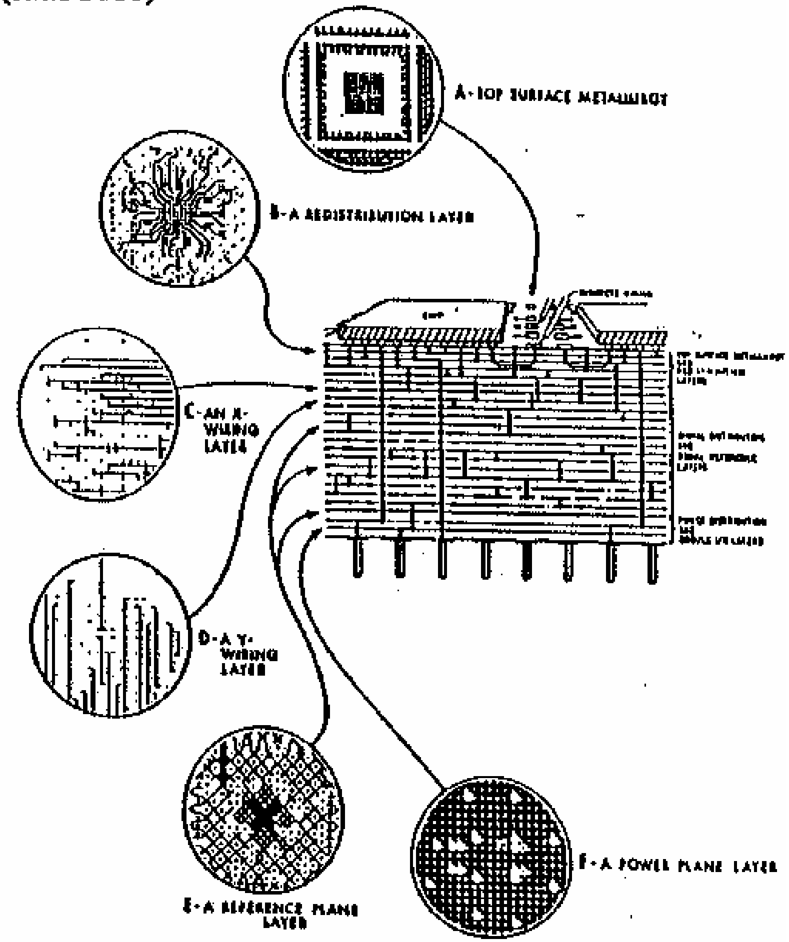


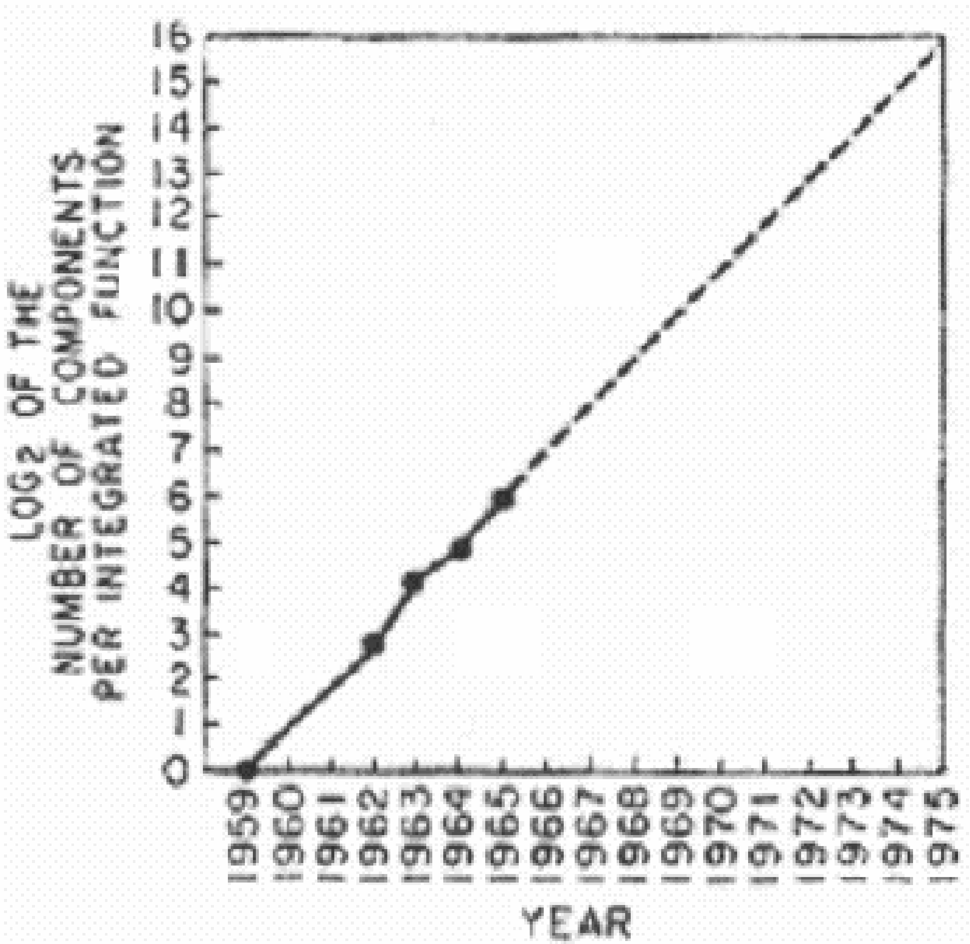
FIGURE 1-4
A high performance multichip module that takes the place of both single chip modules and cards and contains up to 100 chips. Special cooling is required due to the high density.

(IBM 3080)



MLC CONSTRUCTION DETAIL

Moore's Law for Semiconductors



G.E.Moore, Electronics **38** (1965)

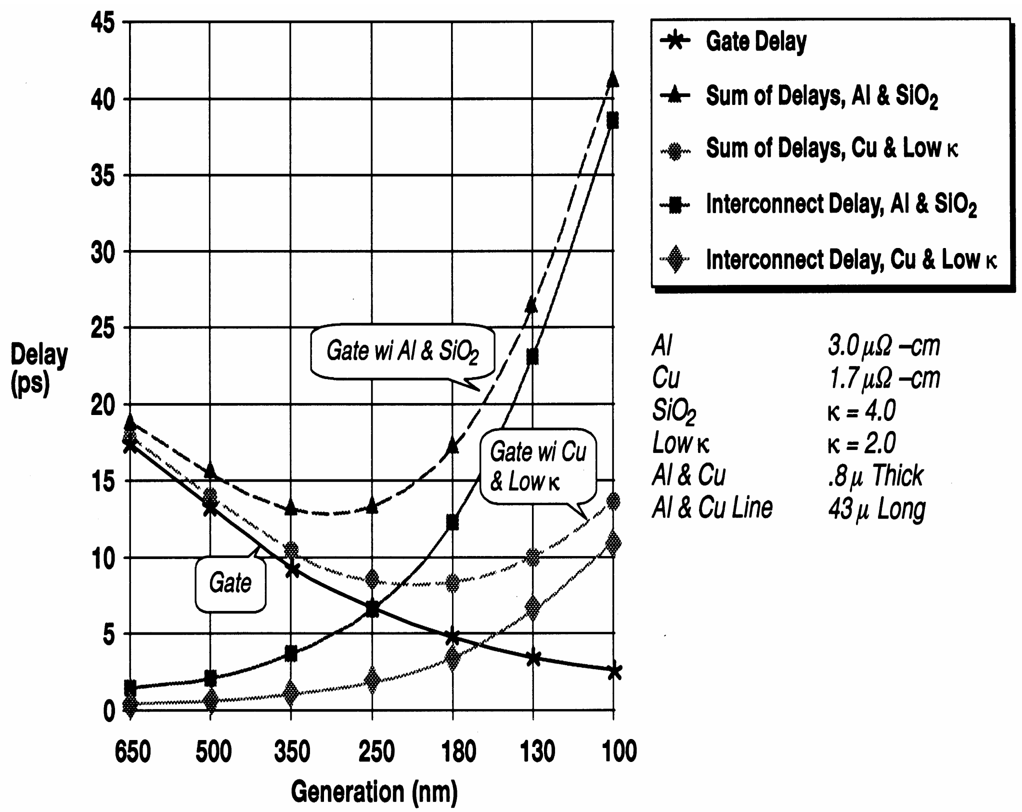
Function

Performance

Cost

Effect of Scaling on Gate and Interconnect Delays

- Interconnect delay dominates IC speed
- Implementation of low k dielectrics reduces
  - RC delay
  - Power dissipation
  - Crosstalk noise
  - Number of metal level



Mark Bohr, IEEE IEDM Proc. 1995

Table 1: Technology Trends and the Need for Low-Dielectric Constant Materials

Year	1995	1998	2001	2004	2007
Feature Size (μm)	0.35	0.25	0.18	0.13	0.10
Metal Levels	4 - 5	5	5 - 6	6 - 7	7 - 8
Device Frequency (MHz)	200	350	500	750	1,000
Interconnect Length (m/chip)	380	840	2,100	4,100	6,300
Capacitance (fF/mm)	0.17	0.19	0.21	0.24	0.27
Resistance (metal1)(ohm/μm)	0.15	0.19	0.29	0.82	1.34
Dielectric Constant (*k*)	4.0	2.9	2.3	<2	2 - 1

- Based on the National Technology Roadmap for Semiconductors, 1994

Interconnects Technology Requirements for MPU

Year of introduction "Technology Node"	2001 130nm	2002	2003	2004 90nm	2005	2006	2007 65nm
MPU ½ pitch	150	130	107	90	80	70	65
Minimum metal effective resistivity (μΩ-cm) Al wiring*	3.3	3.3					
Minimum metal effective resistivity (μΩ-cm) Cu wiring*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Barrier/cladding thickness (conformal) (nm)	16	14	12	10	9	**8**	**7**
Interlevel metal insulator- effective dielectric constant (κ)	3.0-3.6	3.0-3.6	3.0-3.6	**2.6-3.1**	**2.6-3.1**	**2.6-3.1**	**2.3-2.7**

Solutions Exist
Manufacturing Solutions known
No Known Solutions

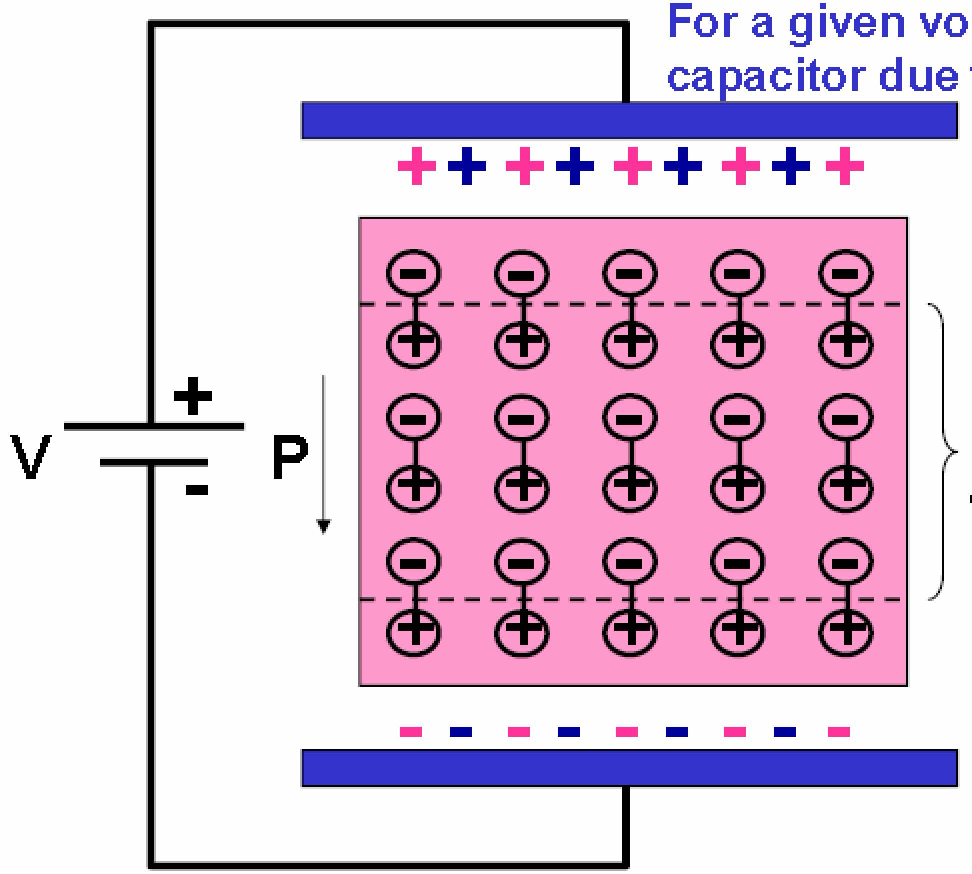
International Technology Roadmap for Semiconductors, 2003

Dielectric Constant

R.P. Feynman et al., The Feynman Lectures in Physics, Addison-Wesley, 1964

For a given voltage, there is additional charge on capacitor due to polarization of the dielectric

The dielectric constant is the factor by which charge on plate is increased (or electric field decreased) compared to free space



No net charge

Polarization

$$\sigma_{plate} = \varepsilon_0 E + P$$

$$P = \varepsilon_0 \chi E$$

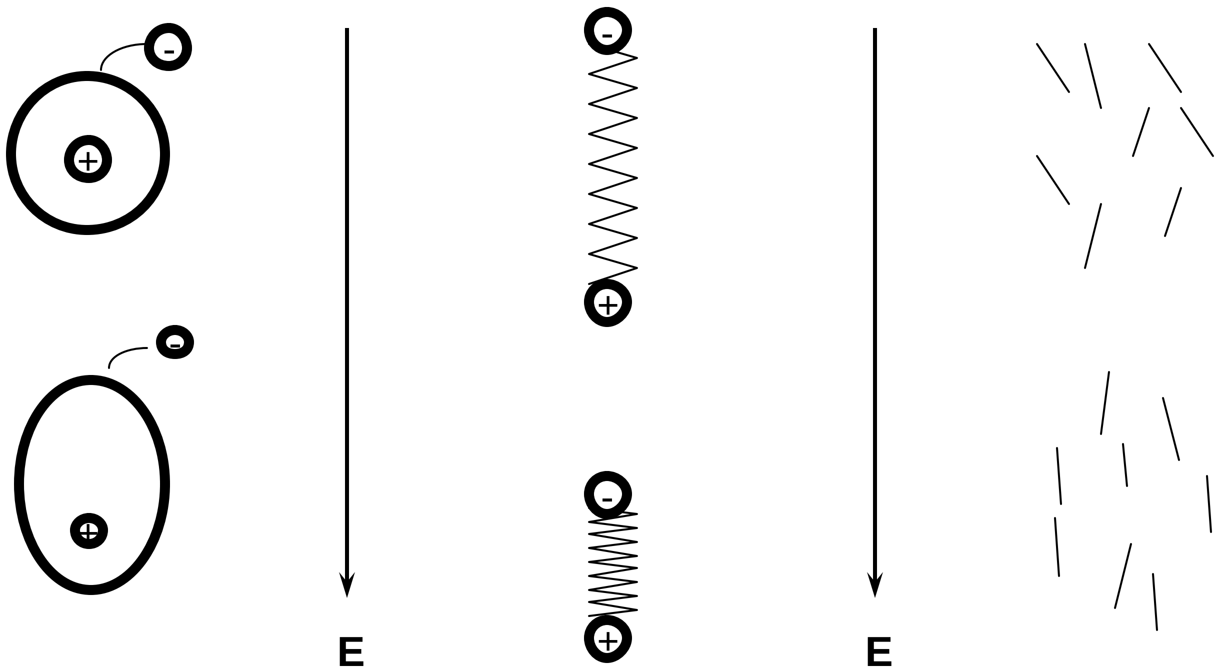
electrical susceptibility

Dielectric constant

$$C = Q / V = \varepsilon_0 \kappa A / d \qquad \sigma_{plate} = \varepsilon_0 (1 + \chi) E = \varepsilon_0 \kappa E$$

Microscopic Origins of Polarization

3 Sources of Polarization



Electronic (Induced)

Visible -UV

Atomic (Induced)

Infrared

Orientational (Permanent)

μw - infrared

K. Taylor, IRPS Tutorial 2000

Electronic Polarizability vs. Strength of Chemical Bonds

Bond	*Polarizability* (angstrom^3)*	*Ave. Bond Energy# (Kcal/mole)*
C-C	0.531	83
C-F	0.555	116
C-O	0.584	84
C-H	0.652	99
O-H	0.706	102
C=O	1.020	176
C=C	1.643	146
C≡C	2.036	200
C≡N	2.239	213

* J. Am. Chem. Soc. 1990, 112, p.8533.
# S. Pine, Organic Chemistry 5th ed.(1987).

PTFE: use of bonds with low polarizability

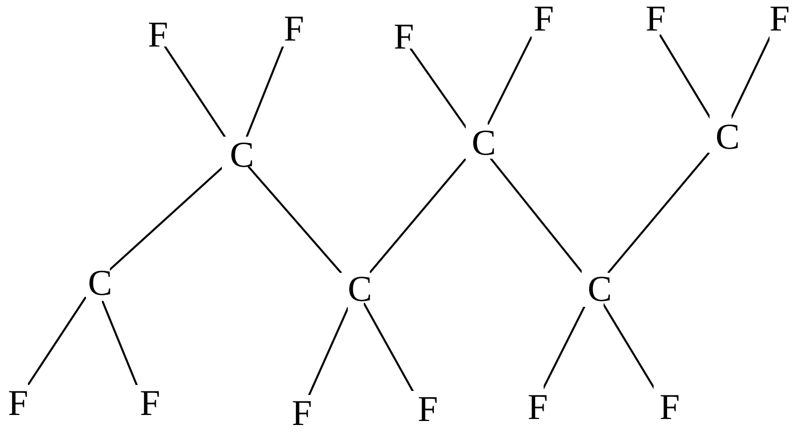
- very low k (~1.9)
- flexible chains limit thermomechanical stability:

  - small modulus

  - low tensile strength

  - low Tg

  - high CTE

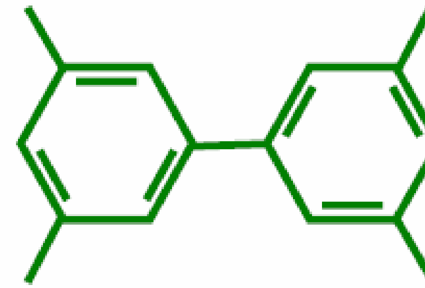


Polymer dielectrics

Spin-on

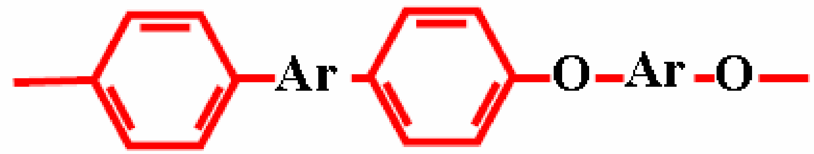
Cross-linked polyphenylene; SiLK™

κ ~ 2.6 (dense) or 2.2 (porous)



Polyarylene; Flare™ κ ~ 2.8

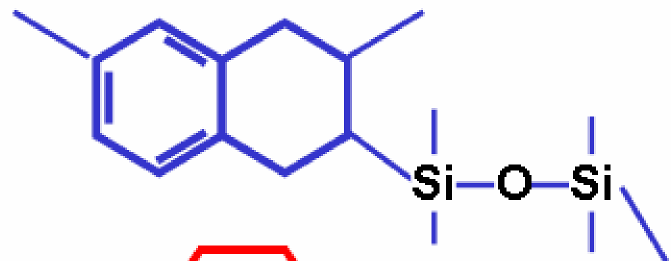
Hardmask FF-02 κ ~ 3.3



CVD

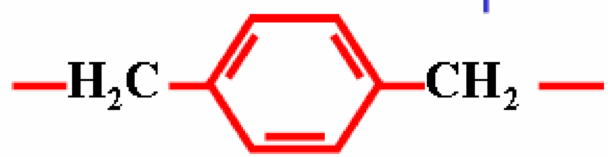
Bis-benzocyclobutene (BCB)

κ ~ 2.8 ; decomposes at 350°C



Parylene N

Pore sealing κ ~ 2.6

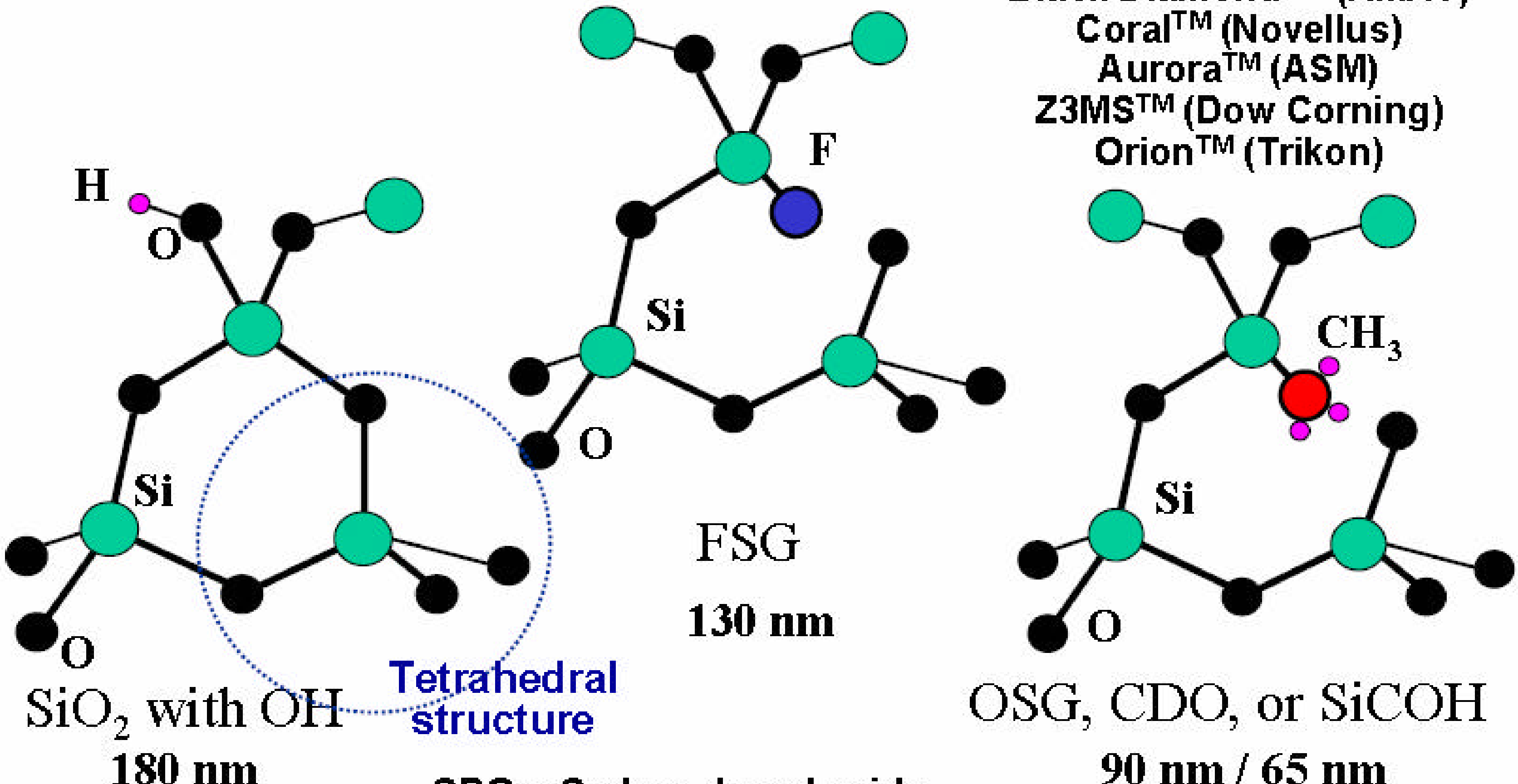


M. Morgen et al., MRS Proc., vol. 565, 1999, p. 69.
N.P. Hacker, MRS Bull., Oct. 1997, p. 33.
A. Das et al., Microelec. Eng., vol. 70, 2003, p. 308.
S.J. Martin et al., Advanced Mater., vol. 12, 2000, p. 1769.

SiO_2 (κ~4.2), FSG (κ~3.6), OSG (κ~2.7)

F or C reduces κ by breaking the SiO_2 network (lower density)

Black Diamond™ (AMAT)
Coral™ (Novellus)
Aurora™ (ASM)
Z3MS™ (Dow Corning)
Orion™ (Trikon)



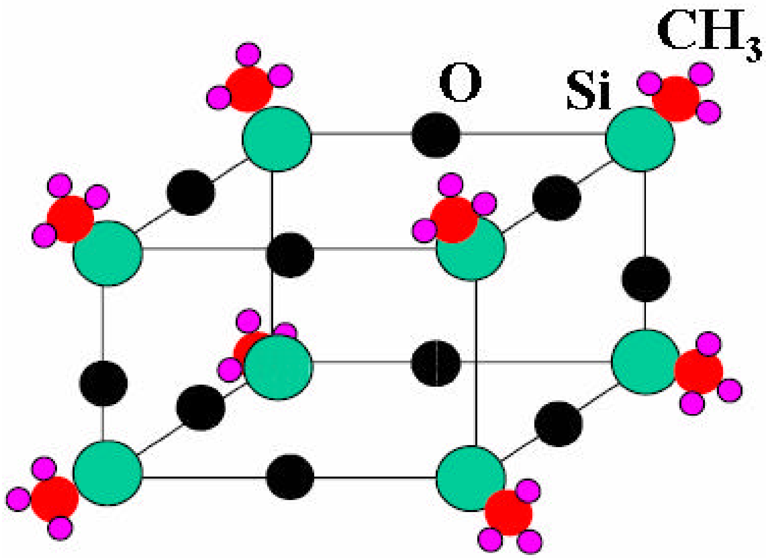
CDO = Carbon-doped oxide
OSG = Organo-silicate glass
FSG = Fluoro-silicate glass

J. Gambino, IEDM Short Course 2004

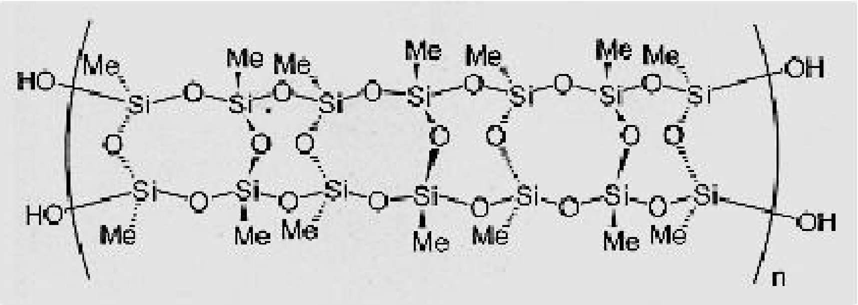
Methylsilsesquioxane (MSQ)

C.T. Chua et al., J. Electrochem. Soc., vol. 149, F9 (2002).
N.P. Hacker, MRS Bulletin, vol. 22, Oct. 1997, p. 33.

Spin-on organosilicate glass $H_3CSiO_{1.5}$ $\kappa \sim 2.7$



T8 cage structure



ladder structure

Honeywell HOSP™; MSQ-based, k i 2.5
JSR LKD-5109; porous MSQ, k i 2.2
Shipley Zirkon™ LK2000; porous MSQ, k i 2.0

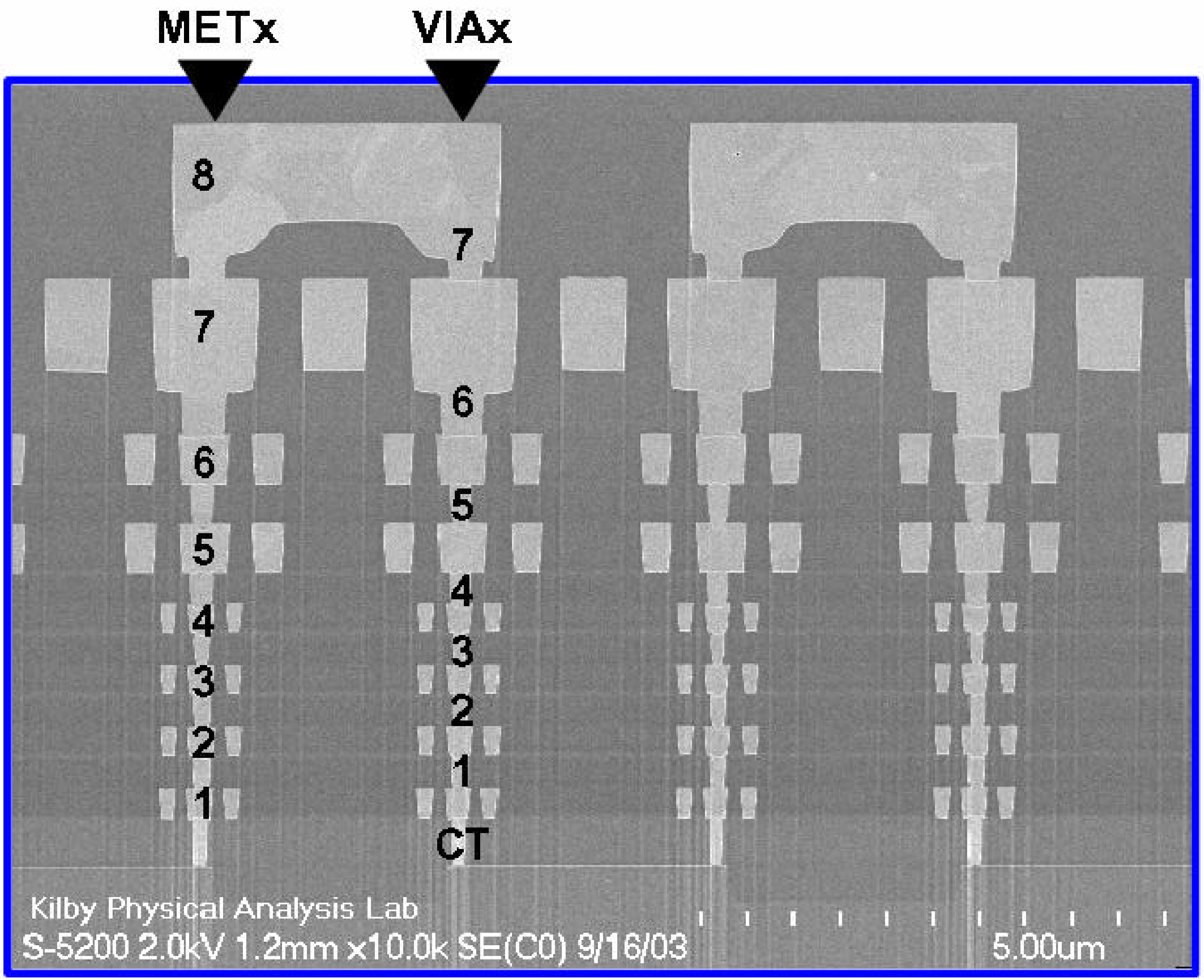
Si-O network provides rigidity
Organic groups lower k to 2.5-3.3

Properties of Low k Dielectrics

Material	deposition	κ	Young's Modulus (Gpa)	Lateral CTE 25 - 225°C (ppm/°C)	T_g (°C)	% wt. loss 425°C 8h	thermal cond. (W/mK)
PTFE	spin-on	1.9	0.5	135	250	0.6	
BPDA-PDA	spin-on	3.1	8.3	3.8	360	0.4	
PAE (crosslinked)	spin-on	2.8	2.7	52	350	2.5	
PAE (fluorinated)	spin-on	2.6	1.9	52	>400	NA	
SiLK	spin-on	2.6	2.3	54	none	2.1	0.18
BCB	spin-on / CVD	2.6	2.2	62	none	30	
Parylene-N	CVD	2.6	2.9	55-100	425 (T_m)	30	
Parylene-F	CVD	2.2	4.9	33	none	0.8	
porous silica	spin-on	2.1	8	NA	NA	NA	
HSQ	spin-on	2.8	7.1	20	none	NA	
OSG	CVD	2.8	10	10	> 450	NA	0.3
FSG	CVD	3.6	60	1.1	>1000	~0	1
SiO2	CVD	4.2	60	1.1	>1000	~0	1

M. Morgen et al. , JOM, Sept. 1999, p. 37.
J. Gambino et al., Proc. IPFA Conf., 2002, p. 111.

TI 90nm Technology: Cu/OSG/SiCN



Cu
FSG(k=3.6)
SiN(k=6.8)

Cu
OSG (k=2.9)
SiCN (k=4.8)

A. McKerrow, Stress Workshop (2004).

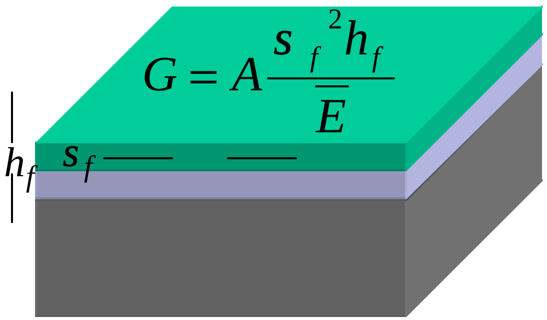
Mechanics of Dielectric Cracking & Interface Delamination

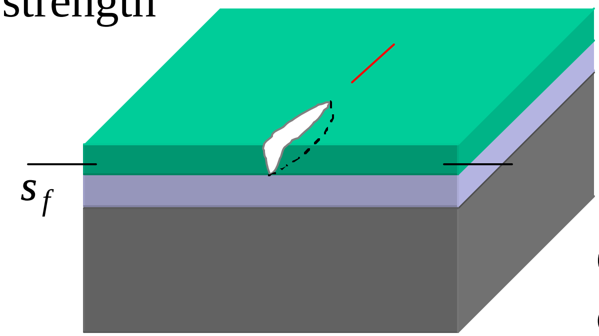
$$G - \Gamma$$

Crack driving force

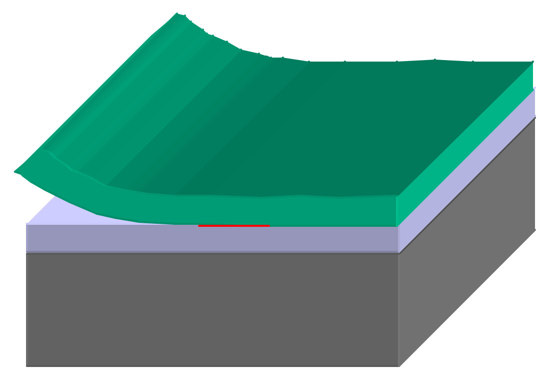
Cohesive strength

Release of strain energy





Cohesive cracking



Interface debonding

Crack or debonding driving force is measured by the strain energy released per unit area: Strain energy release rate (ERR), or ***G***

Material resistance against cracking is defined as cohesive strength Γ, related to the fracture toughness K_I and modulus E in K^2/E

Stress Generation in Low k Structures

Processing induced stresses

- Film deposition
- Thermal process

Thermal stresses

- Thermal and elastic mismatch of dissimilar materials

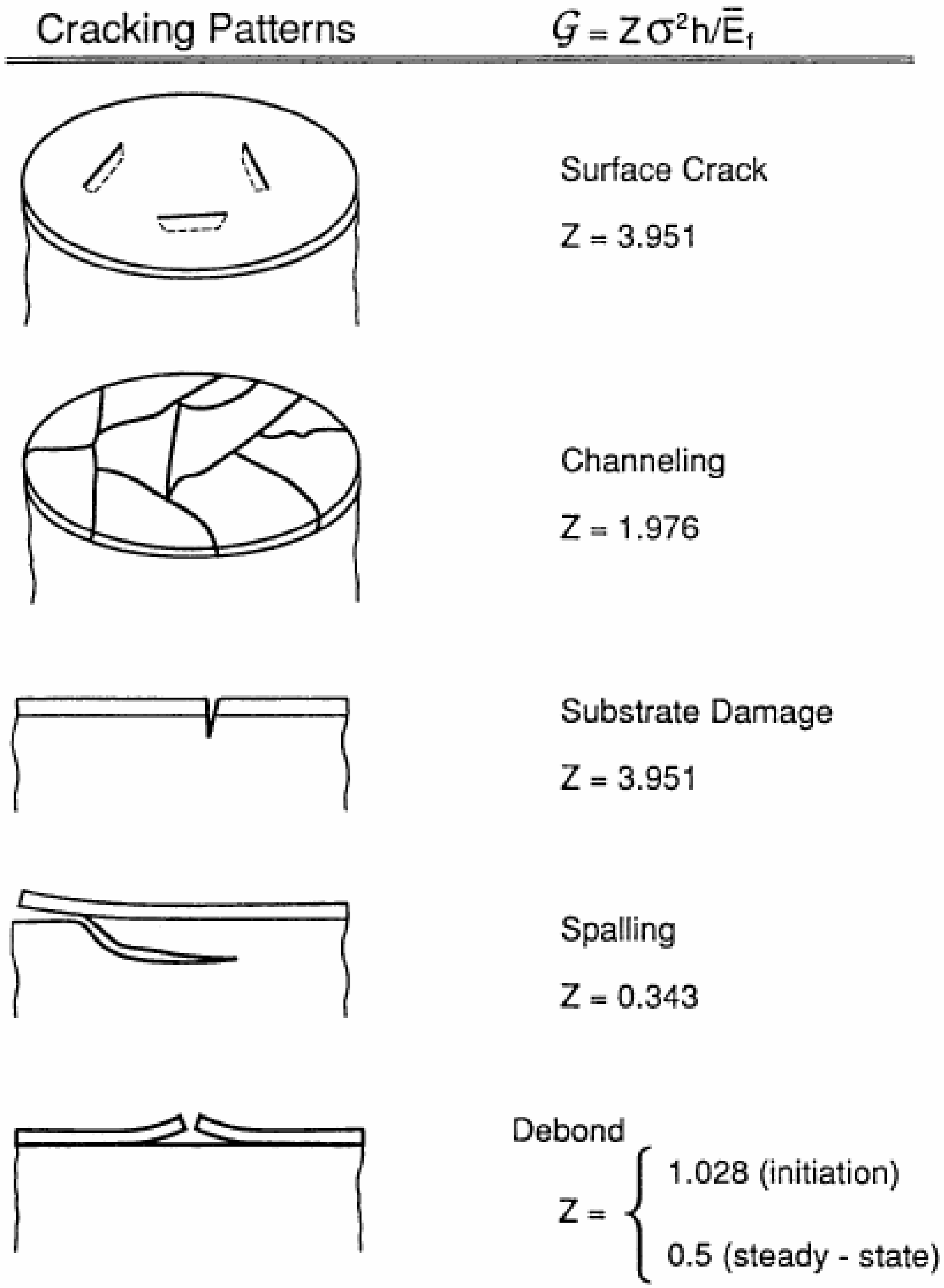
Electromigration induced stresses

- Current induced mass transport

Packaging assembly stresses

- Package deformation during assembly, depending on materials, interconnect geometry & dimension, assembly process

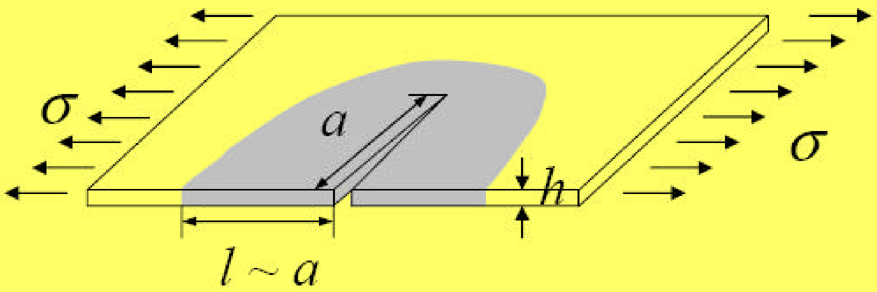
Low k is weak – Impact on reliability?



Crack formation in films in tension. The driving force G is deduced assuming elastic and homogeneous film and substrate and infinitely thick substrate.

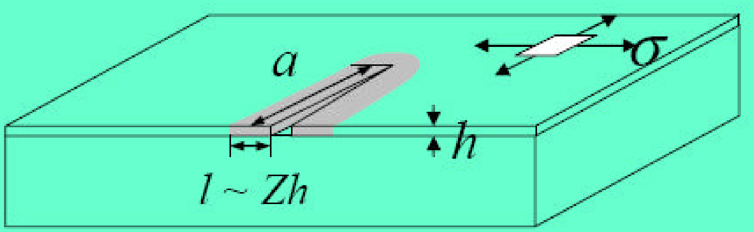
Hutchinson & Suo, Advances in Applied Mechanics, 29, 64-192, 1992.

Effect of Substrate Confinement



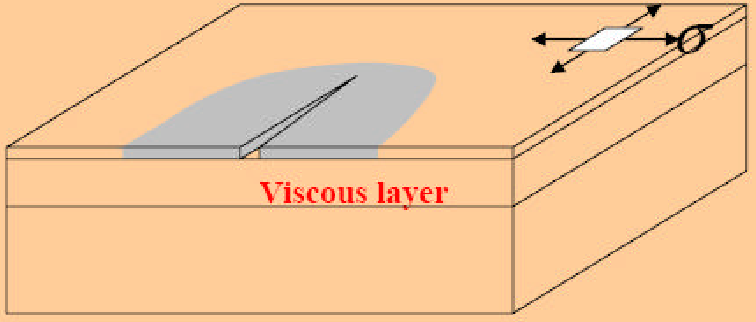
Free-standing film

$$G \sim \frac{\sigma^2}{E} a$$



Film on elastic substrate

$$G \sim \frac{\sigma^2}{E} l$$

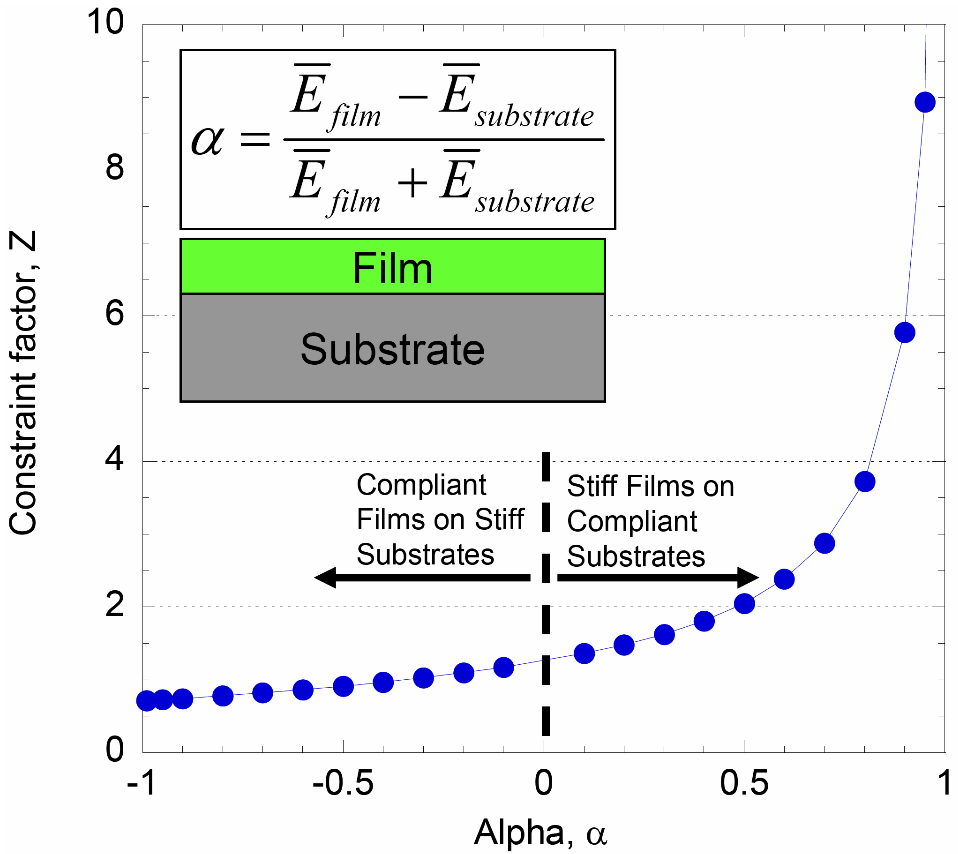


Film on viscous layer

Gradual loss of constraint

Z. Suo, IRPS Tutorial 2006

Constraint Factor Z

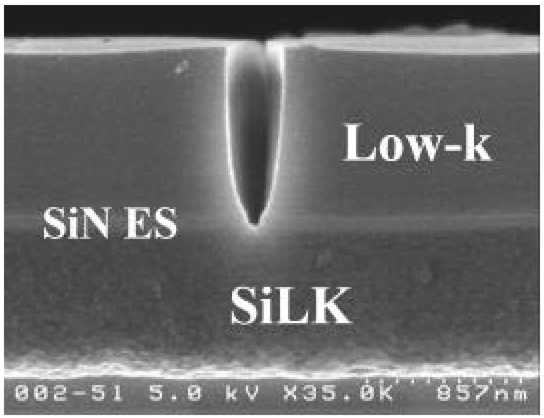


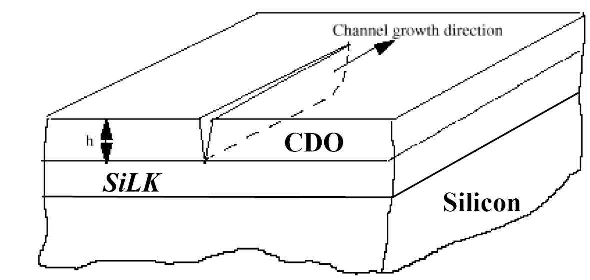
T. Tsui *et al.* (TI), MRS, Spring 2005

Effects of elastic mismatch on Z

A function of thermal mismatch, elastic mismatch, underlayer plasticity, geometry, flaw size and location.

Cracking Induced by Compliant Substrate Films in Organic/Inorganic Hybrid Structures





$$G_{ss} = Z \frac{s_f^{\,2} h_f}{\overline{E}}$$

$$Z_{total} = Z_{elastic} + Z_{plastic}$$

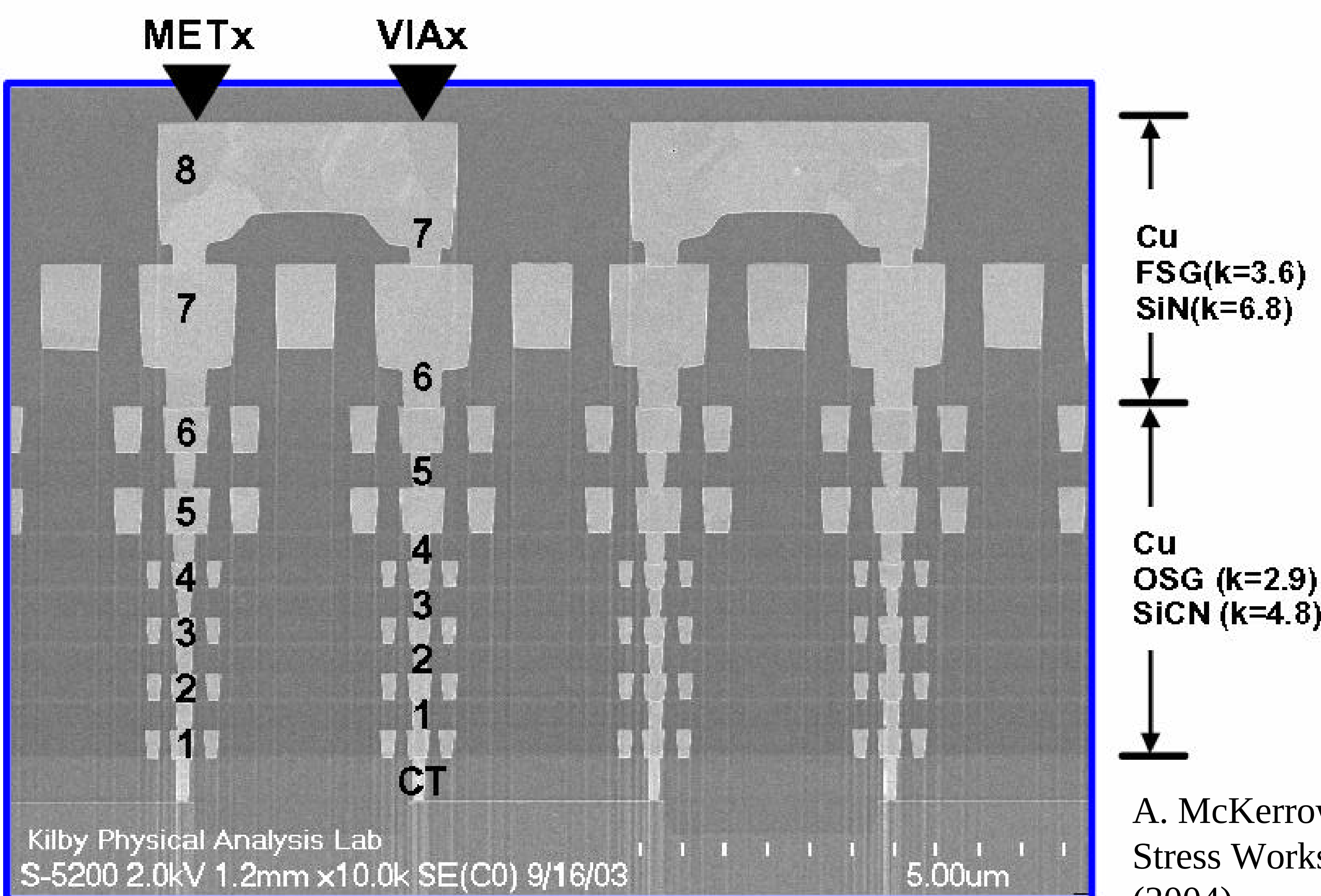
$$= f\left(E_1, E_2, u_1, u_2, geometry\right) + \boxed{\frac{s_f}{\sqrt{3} s_Y}}$$

~ 0.5 for CDO/SiLK

J. He *et al.* (Intel), 7th Stress Workshop, 2004

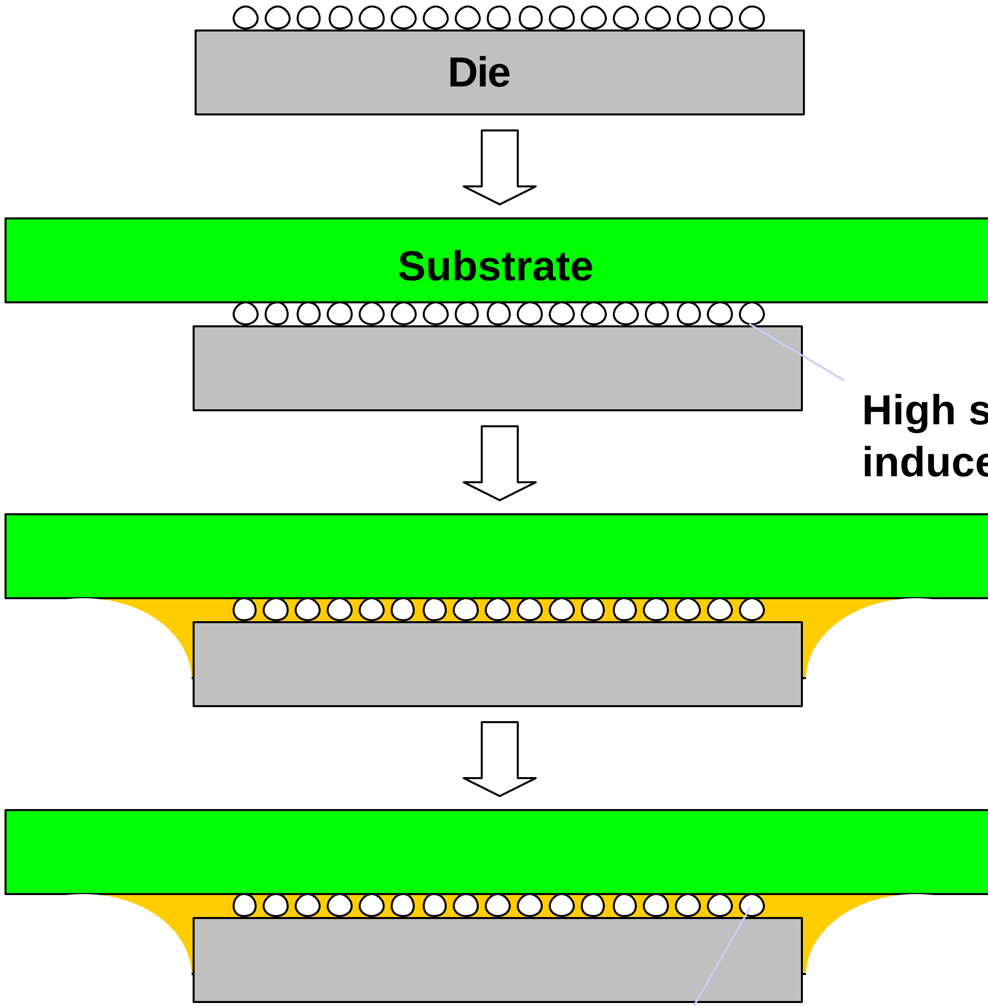
Elastic mismatch and underlayer plasticity can increase the crack driving force in the brittle ULK overlayer.

TI 90nm Technology: Cu/OSG/SiCN



A. McKerrow, Stress Workshop (2004).

Flip-Chip Packaging



Solder bumping

Solder reflow
183^{o} C 37Pb/63Sn

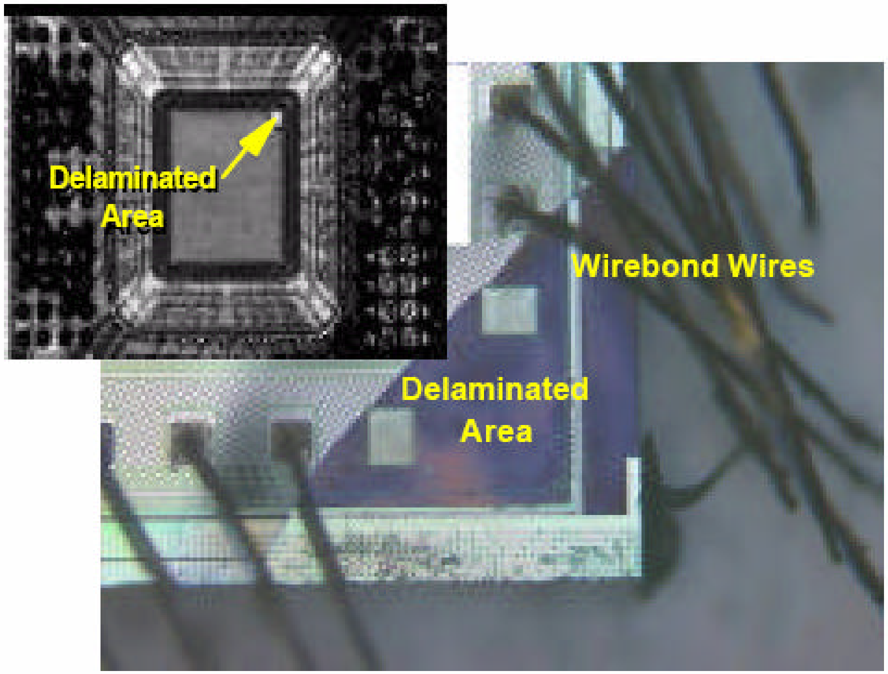
High stress in the package induced by the die attach process

Underfilling
125^{o} to 180^{o}C

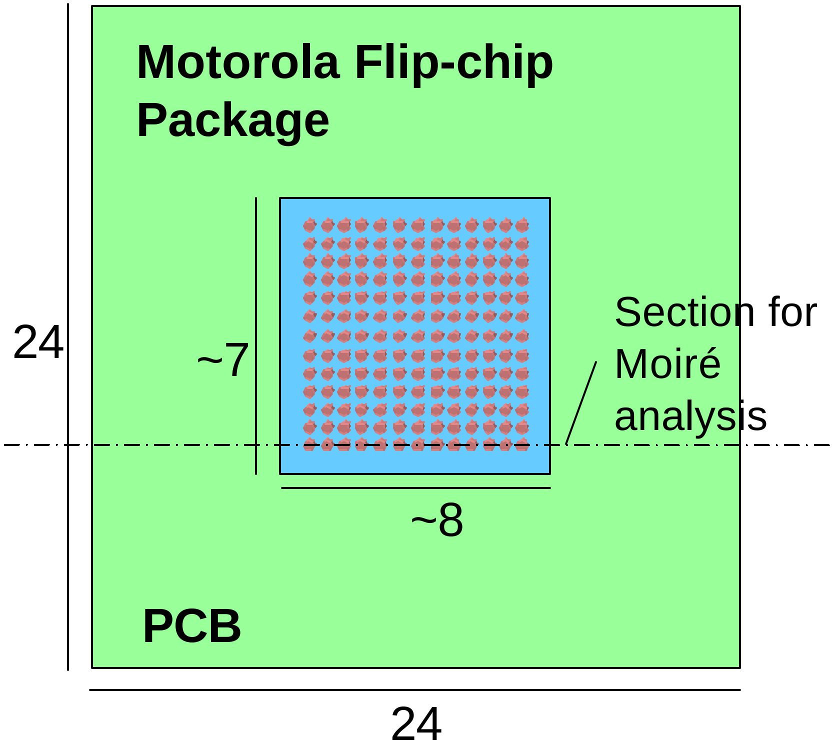
Thermal cycling
-55^{o}C-125^{o}C

High stress due to thermal cycling.

Chip-Package Interaction

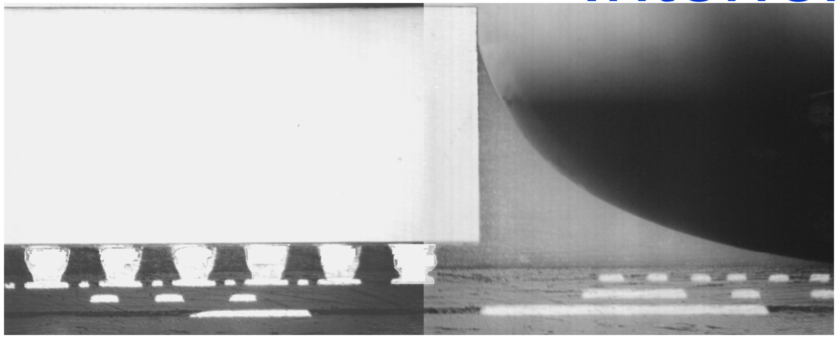


PBGA Wirebond CSAM and Failure Analysis
W. Landers et al., IITC 2004



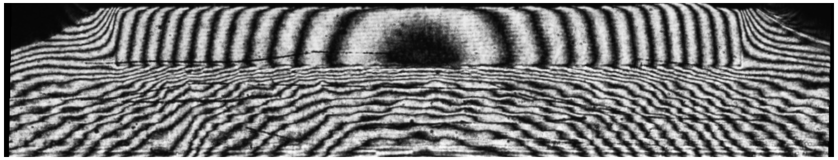
Plastic flip-chip package for
moire analysis

Package Deformation Measured by Moiré Interferometry

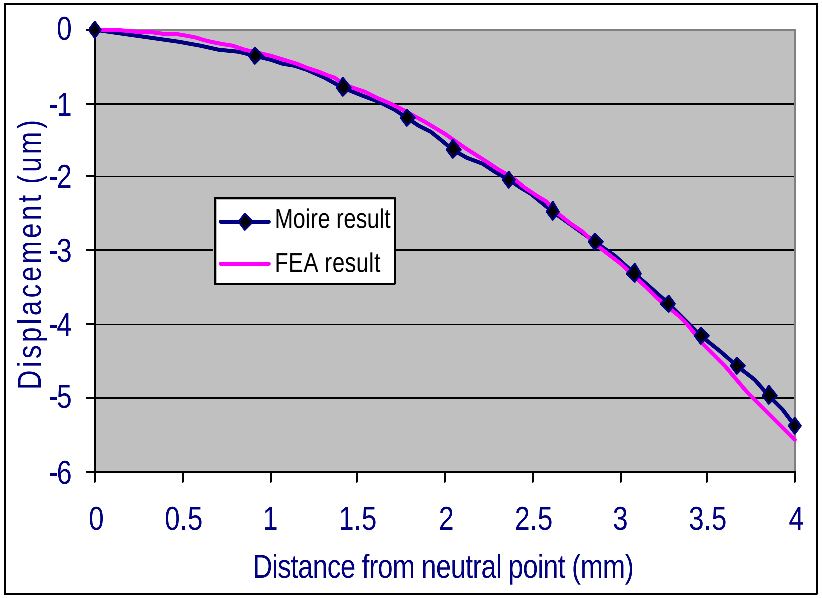


Package cross-section

U Field



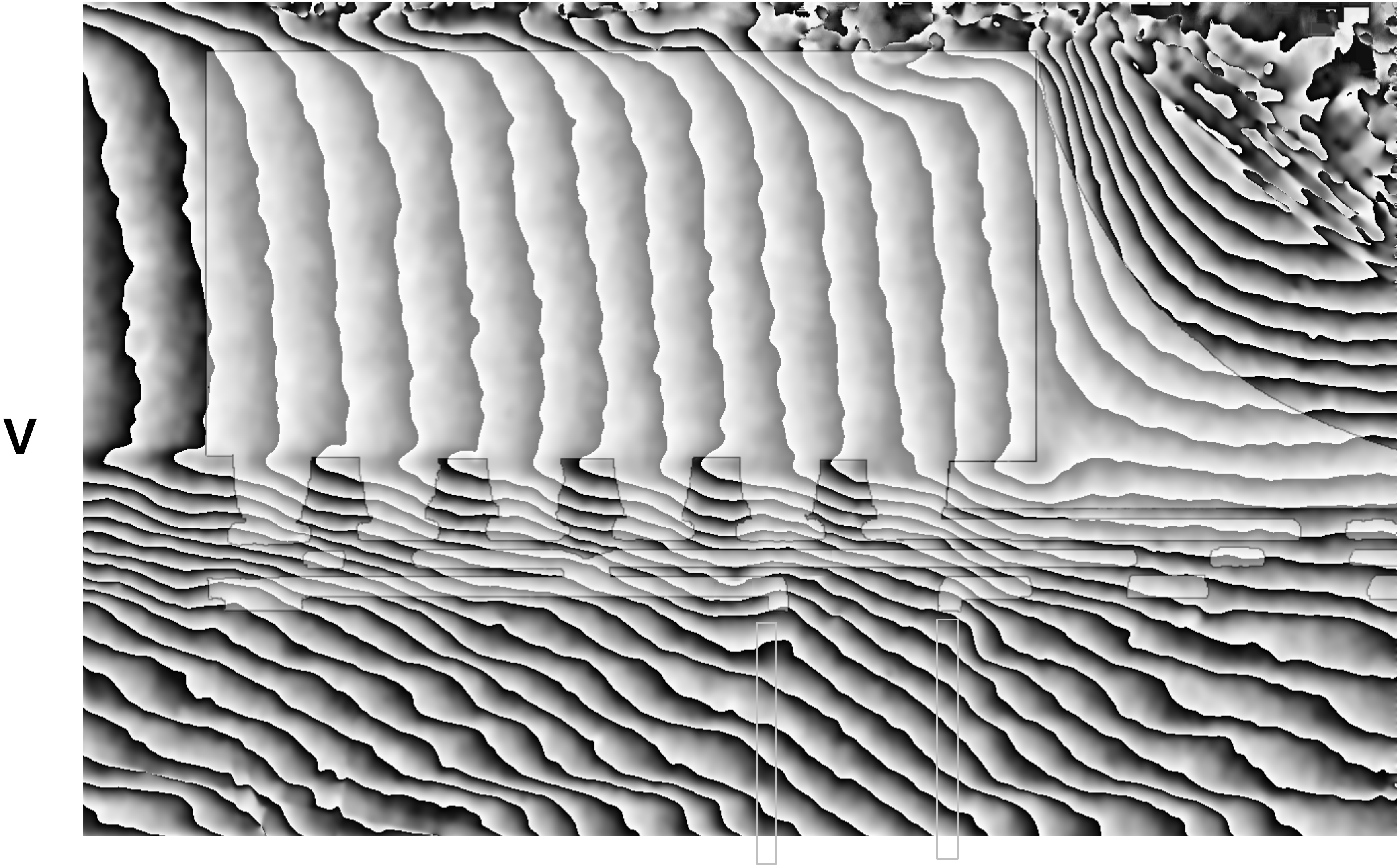
V Field



Package warpage

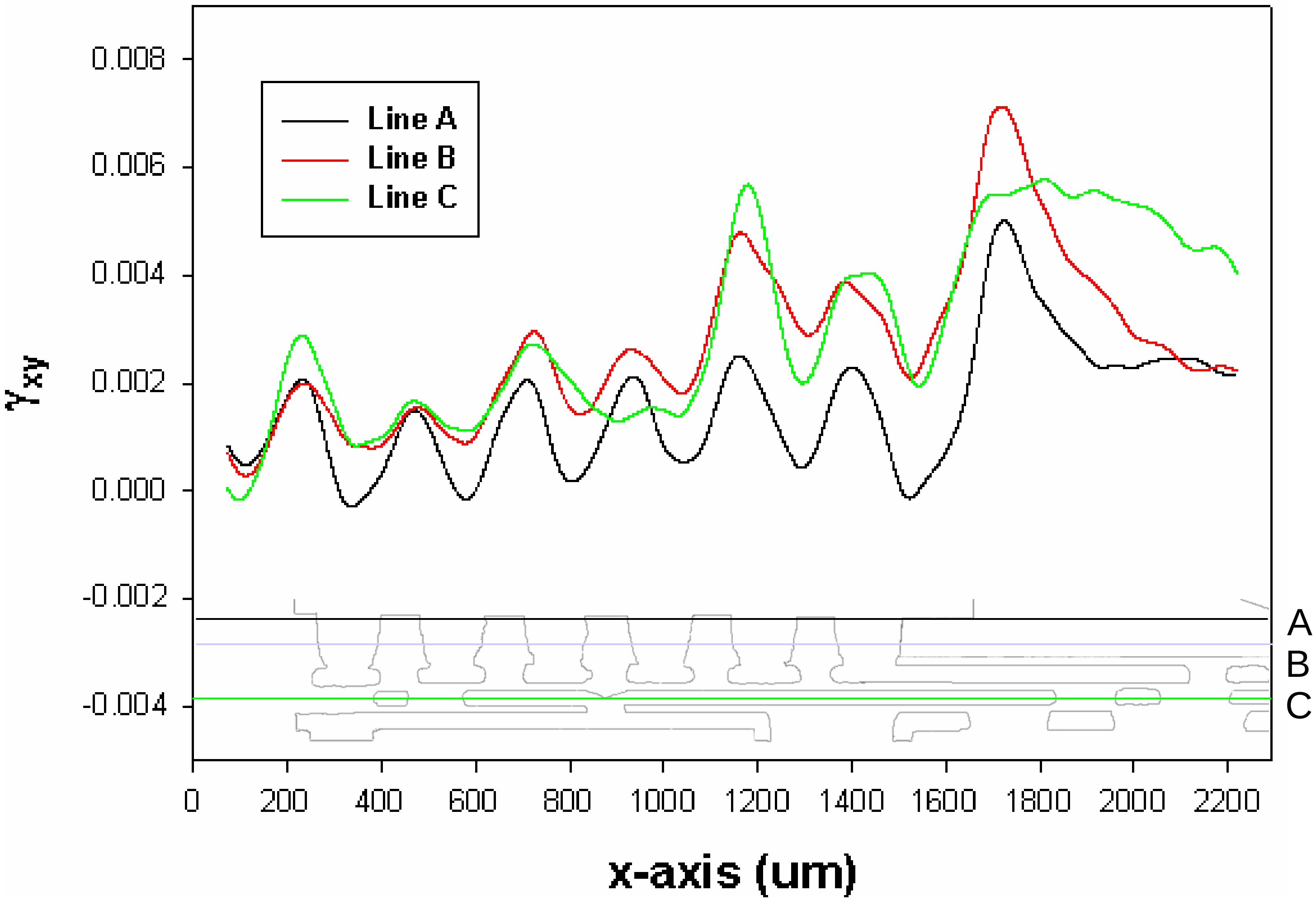
High resolution moiré interferometry was used to measure the thermal deformation in the flip-chip package and verified the modeling results at the package level.

High Resolution Phase Map



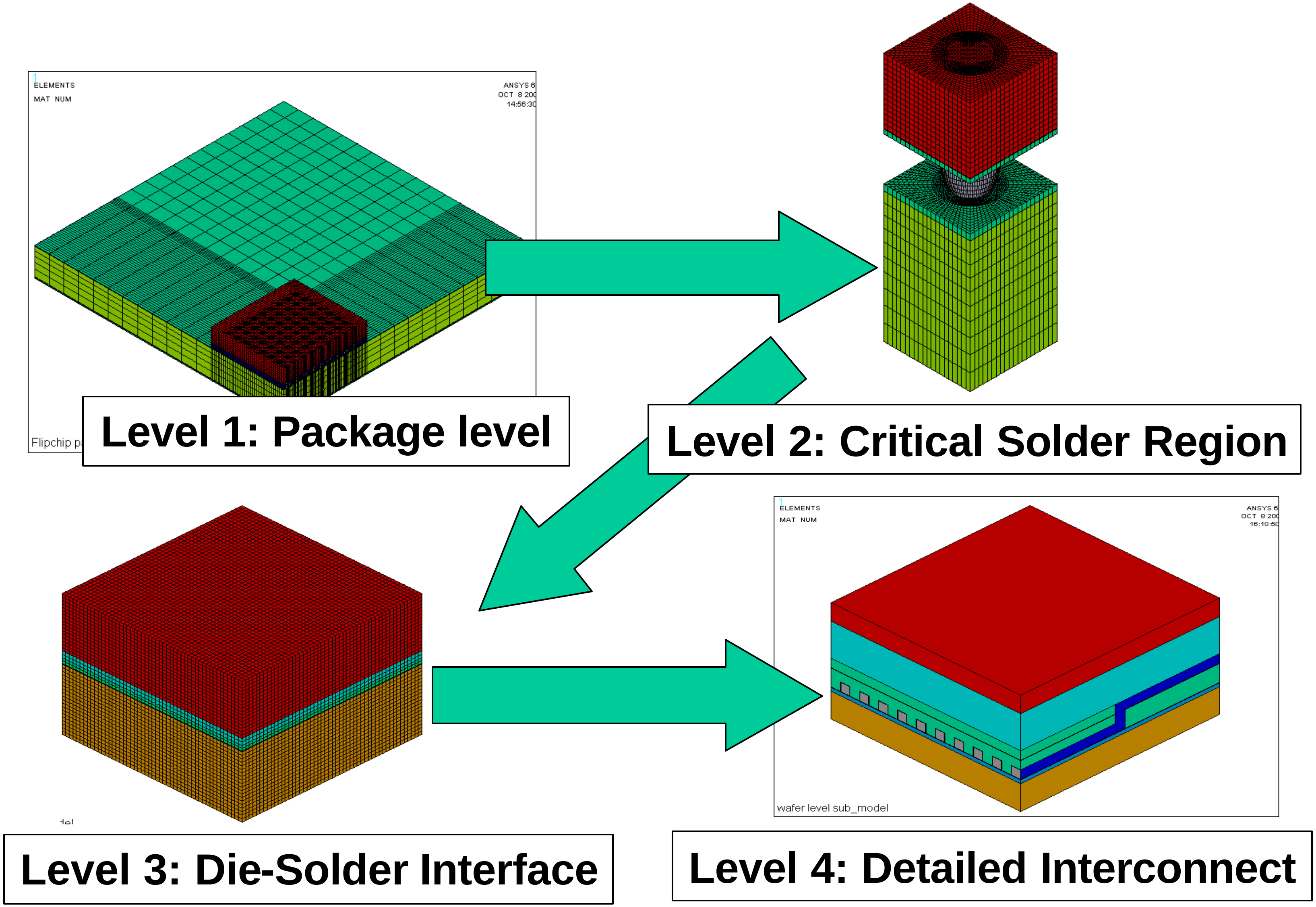
Thermal load -80°C; Fringe spacing 208 nm (Ho et al., Micro. Reliab. ’04)

Shear Strain Distribution



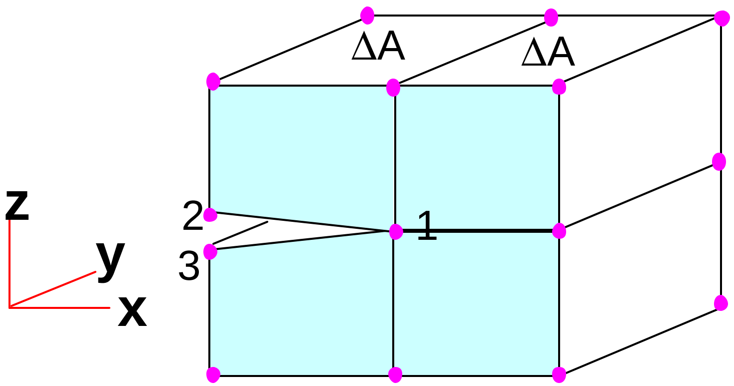
Warpage introduces shear and peeling strains up to 0.5% for thermal load of -80°C. Strains of 3x can be reached during die attach, depending on the solder reflow temperature.

3D Multi-level Sub-model

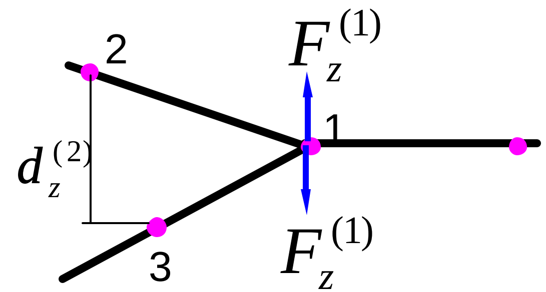


Wang et al., Stress Workshop 2005

MVCC Technique
(Modified Virtual Crack Closure)

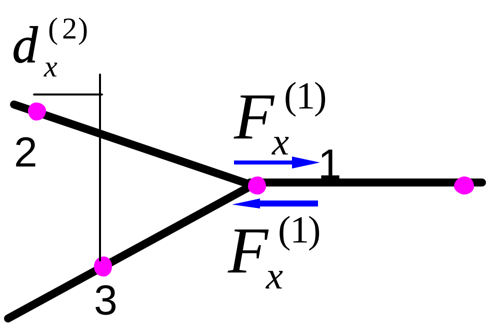


FEA elements and nodes near crack tip



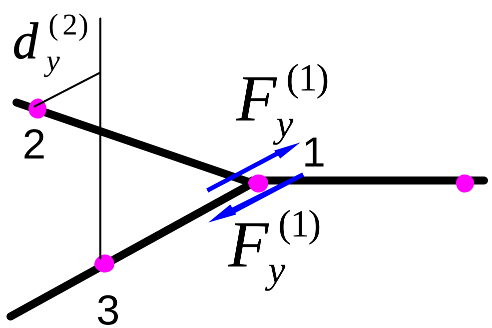
Mode 1 component

$$G_I = F_z^{(1)} d_z^{(2)} / (2\Delta A)$$



Mode 2 component

$$G_{II} = F_x^{(1)} d_x^{(2)} / (2\Delta A)$$



Mode 3 component

$$G_{III} = F_z^{(1)} d_z^{(2)} / (2\Delta A)$$

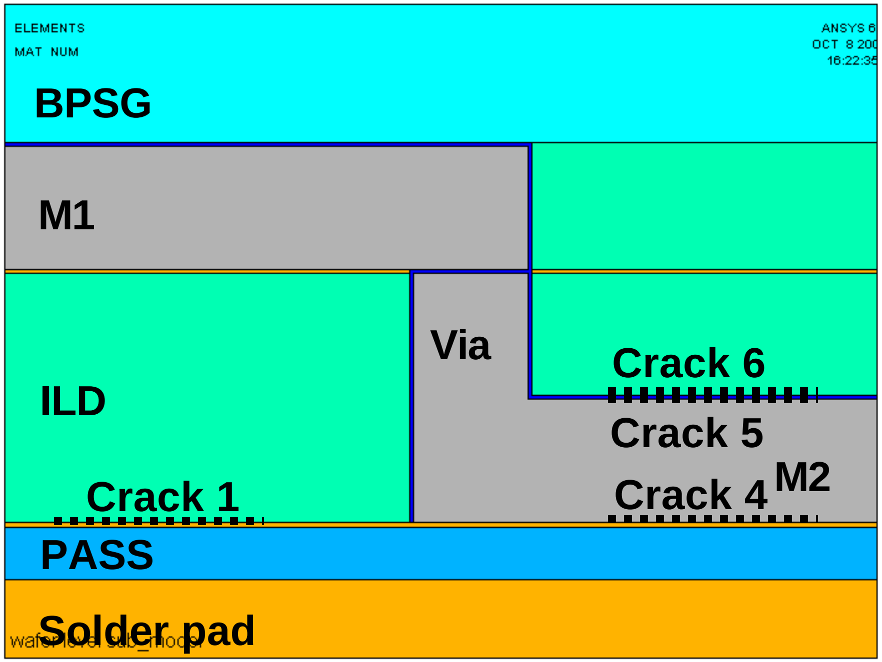
F_X, F_y and F_z are nodal forces at node 1 along x,y and z direction, respectively.

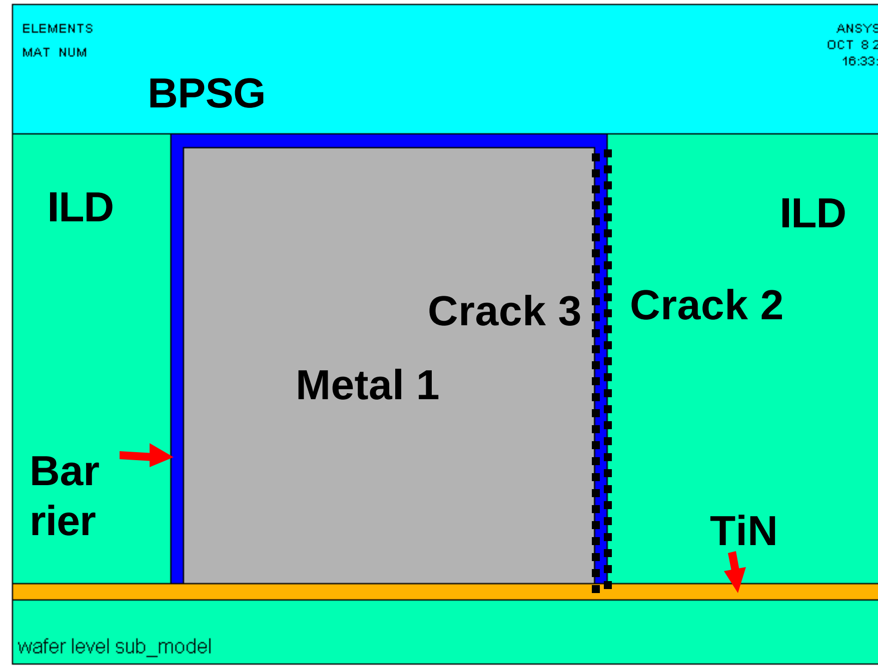
δ_X, δ_y and δ_z are relative displacements between node 2 and 3 along x,y and z direction, respectively.

Total energy release rate: $G = G_I + G_{II} + G_{III}$

The University of Texas at Austin

Interconnect Interfaces

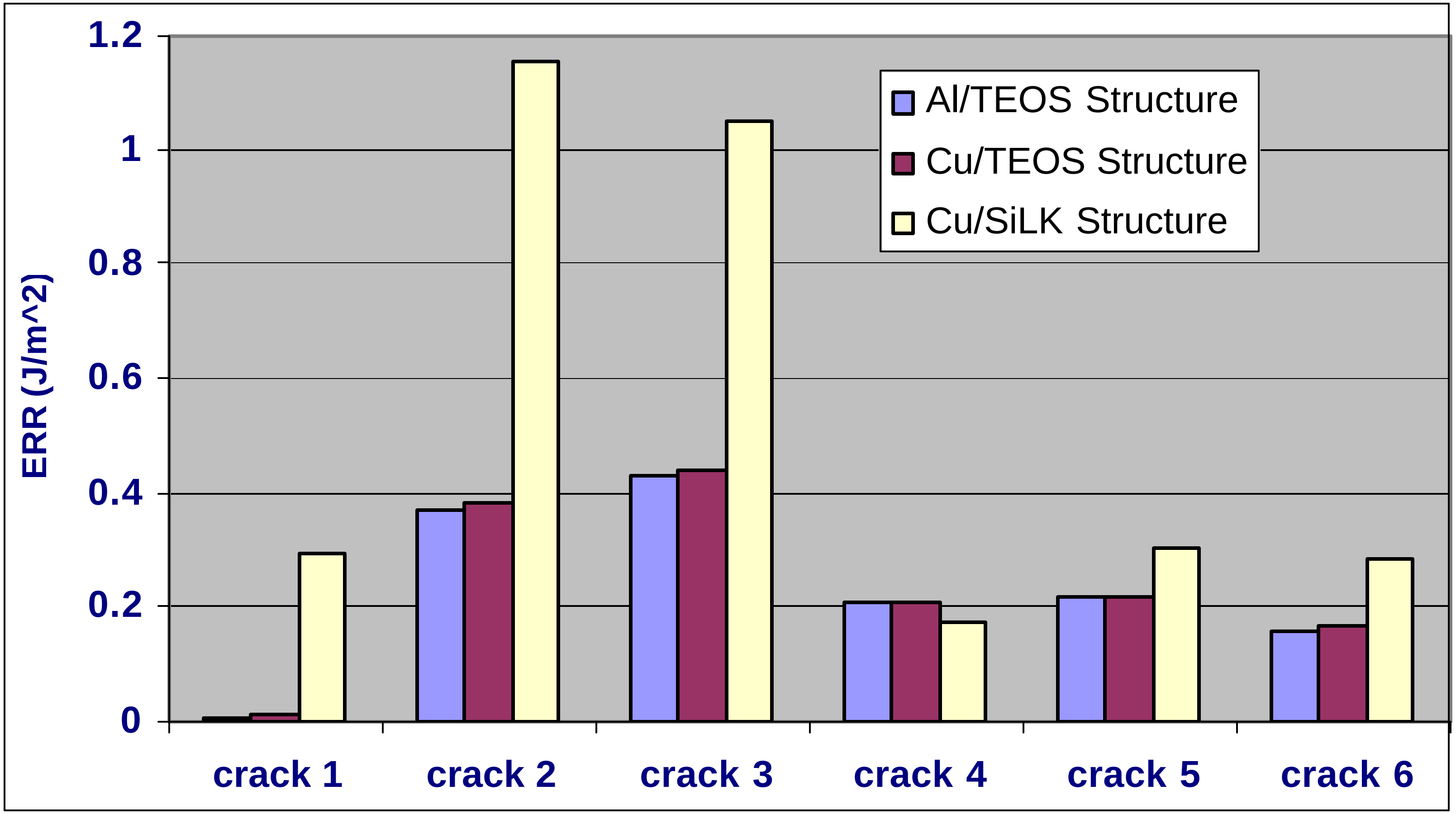




Crack 1,4, 5 and 6 are at the horizontal cap and barrier layer interfaces. Crack width is taken to be the line width. Crack 2 and 3 are at the vertical barrier interfaces.

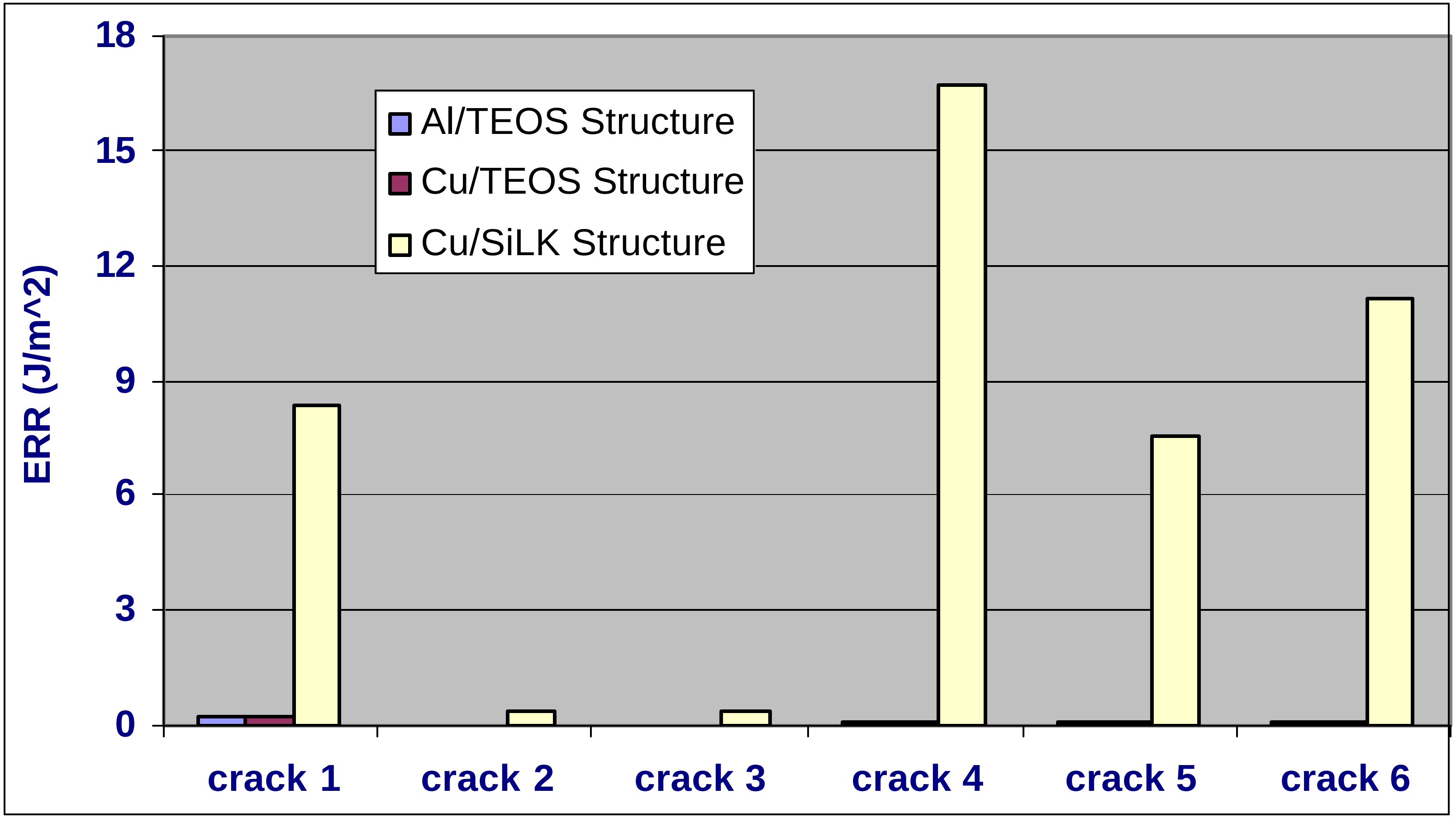
ERR for Stand–alone Wafer Structures

(from 400^{o}C to 25^{o}C)



The SiLK/barrier interface in Cu/SiLK structure has the highest energy release rate (about 1.16 J/m^2). Fracture mode is primarily mode I driven by the high CTE of SiLK.

Packaging effect (-55ºC to 125ºC)



Packaging has a significant effect on energy release rate for Cu/SiLK structure. Mode mixity is dominated by the peeling force corresponding to mode I although shear stresses also contribute.

Why energy release rate is much higher in Cu/low k structure than in Cu/TEOS structure ?

The energy release rate as the crack driving force

$$G = Z\frac{s_f^{\,2} h_f}{\overline{E}}$$

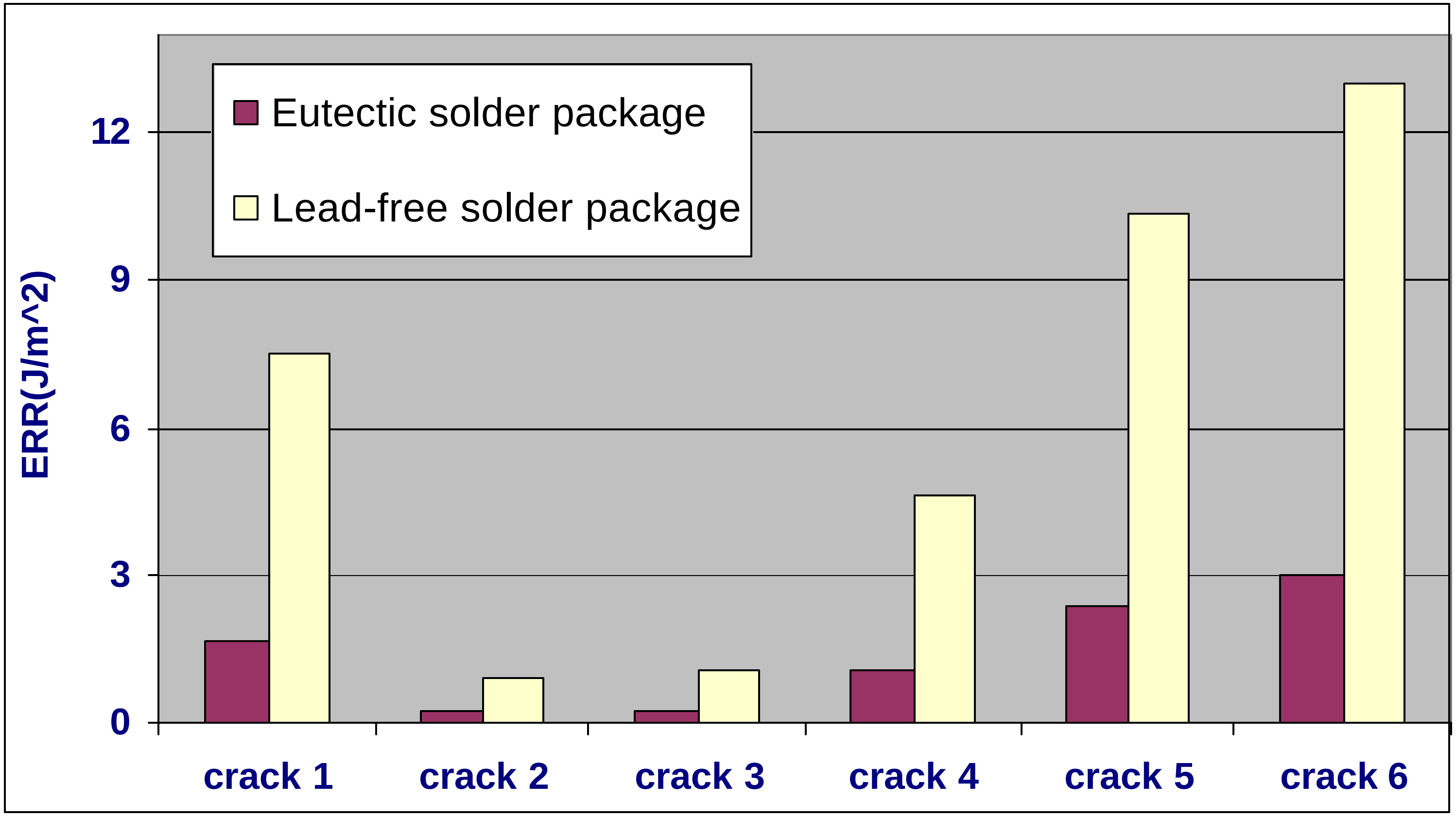
For the same packaging induced stress σ, the strain energy densities are:

$$x_{SiLK} = \frac{1}{2} s e_{SiLK} = \frac{1}{2}\frac{s^2}{E_{SiLK}}$$

$$x_{TEOS} = \frac{1}{2} s e_{TEOS} = \frac{1}{2}\frac{s^2}{E_{TEOS}}$$

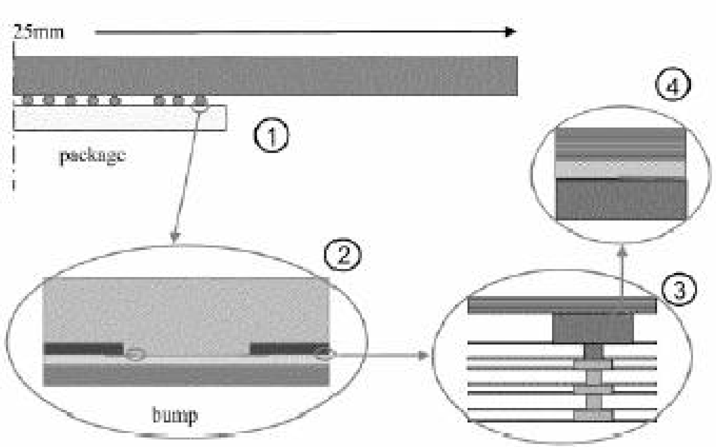
E_{SiLK} is about 30 times lower than E_{TEOS}, hence a much higher energy release rate in the Cu/SiLK structure. Note that for CPI, G depends mainly on E but less on CTE.

Solder Materials Effect
(Cu/MSQ, Plastic substrate, 7x8mm die)



Pb-free solder package is more susceptible to interfacial delamination in Cu/MSQ structures due to a higher reflow temperature but the energy release rate is lower than the Cu/SiLK structure.

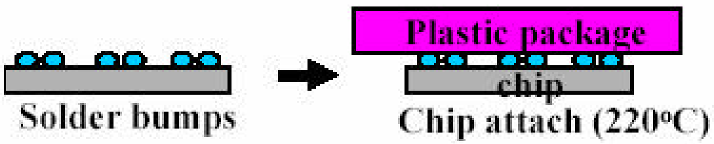
2D Multi-scale Modeling of CPI for Low k Structures

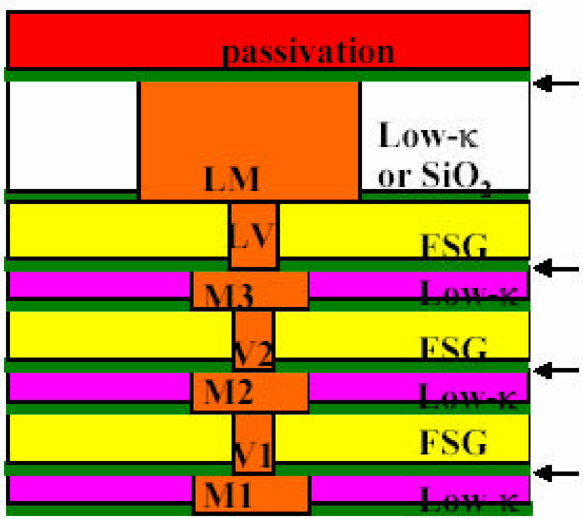


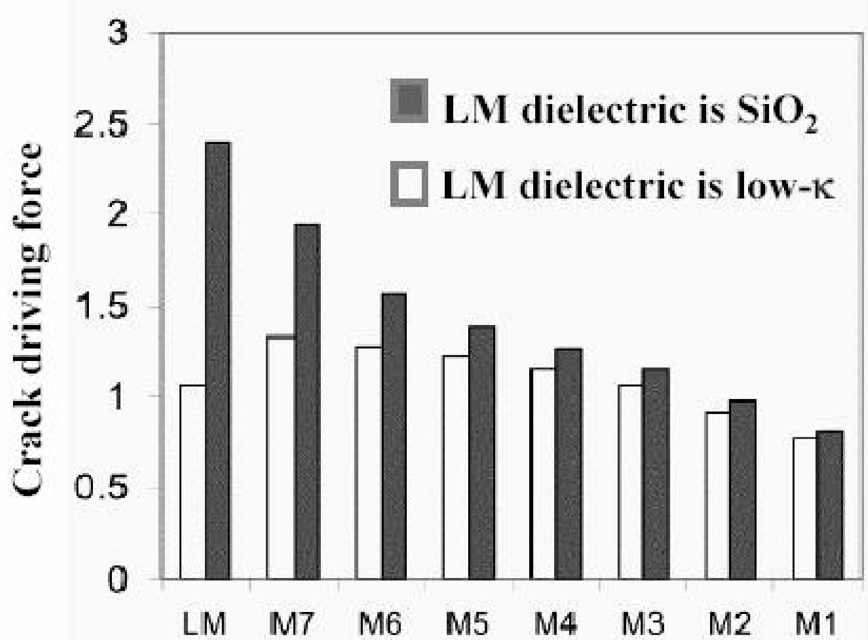
L.I Mercado et al., Elec. Comp. Tech. Conf., 2003, p. 1784
G. Wang et al., IRPS Proc., 2004, p. 557.

Model stress on chip from die attach

- Thermal expansion mismatch between chip and package
- Weakest interface is low-κ / barrier interface
- Highest stress is at top of metal stack
- Maximum stress can be reduced by using SiO_2 as the dielectric for LM







Curing

Thermal cure; 400 – 450 °C, 20 – 60 m

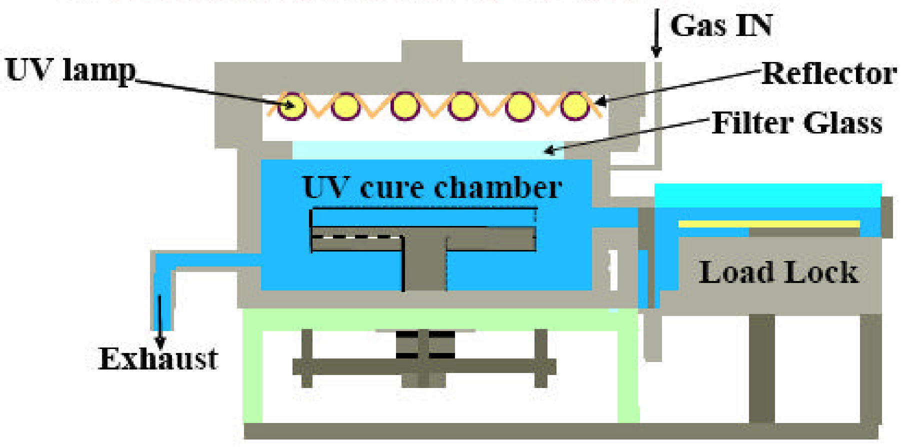
Improves mechanical properties, but high thermal stress on Cu

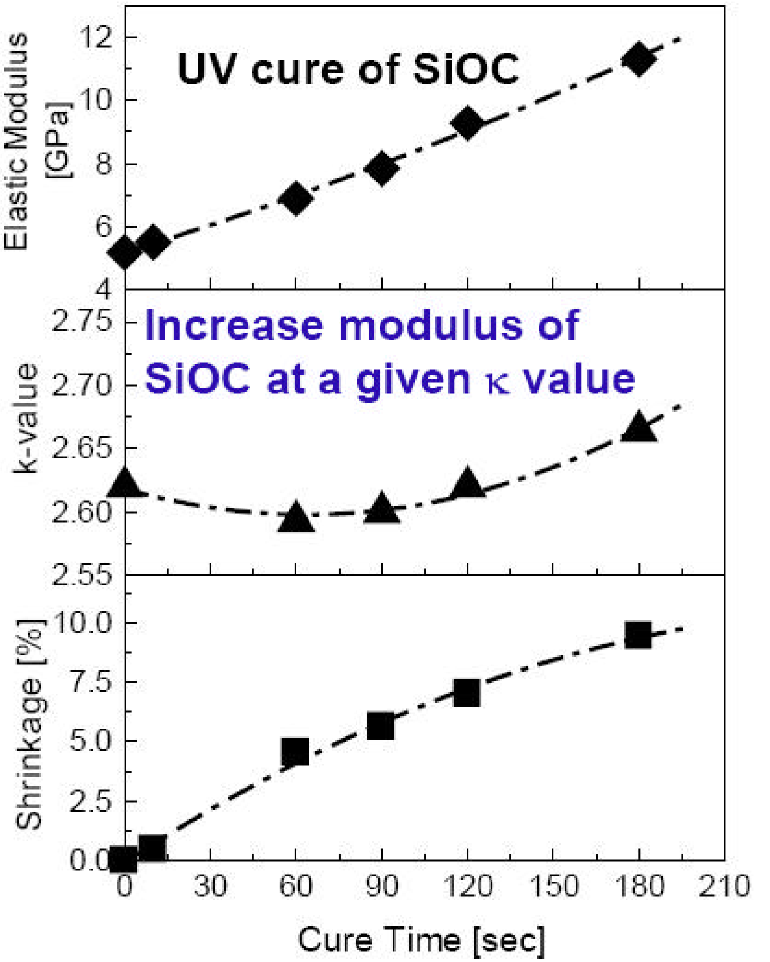
UV cure; 300 - 400 °C, 1 m

E-beam cure; 350 °C, 2 – 12 m

Improves mechanical properties, low thermal stress on Cu

But increased stress in low-k





K. Yoneda et al., IITC 2005, p. 220.

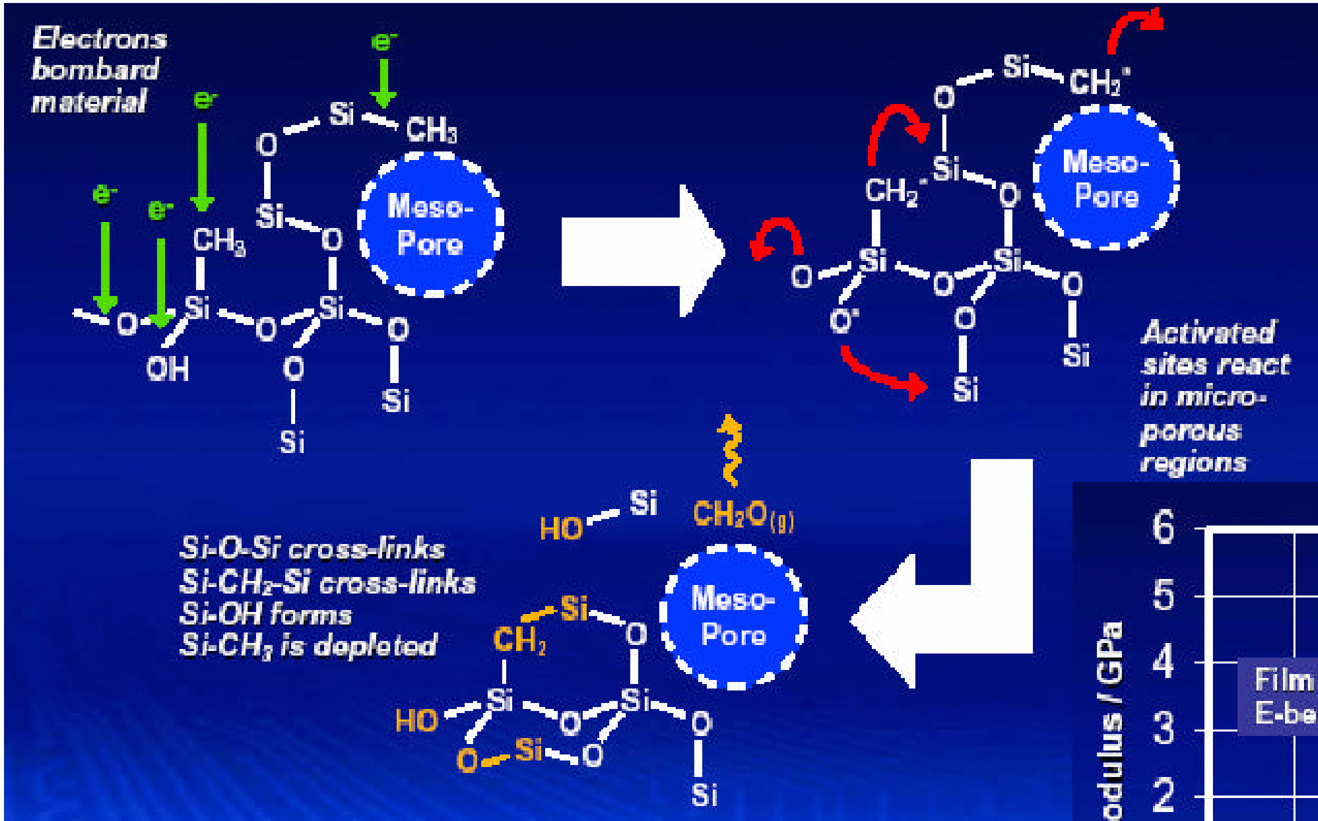
Y. Toivala et al., JECS, 149, F9 (2002).

K. Fujita et al., IITC 2003, p. 106.

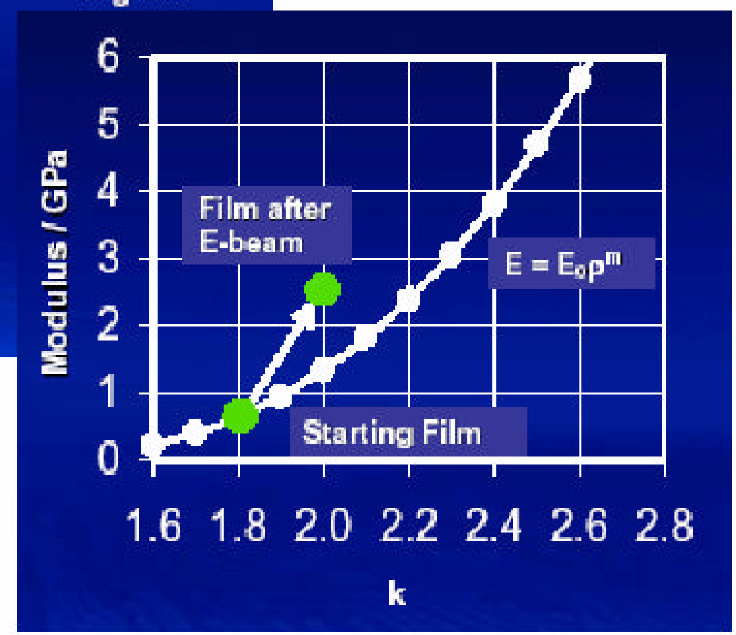
K. Yoneda et al., AMC 2003, p. 483.

F. Iacopi et al., AMC 2005, p. 247.

Mechanism of E-beam Curing



Increase modulus of OSG or a given κ value



G. Kloster et al., IITC Proc., 2002, p. 242.

Interconnect Technology Challenges (ITRS)

Five difficult challenges for >65nm through 2007

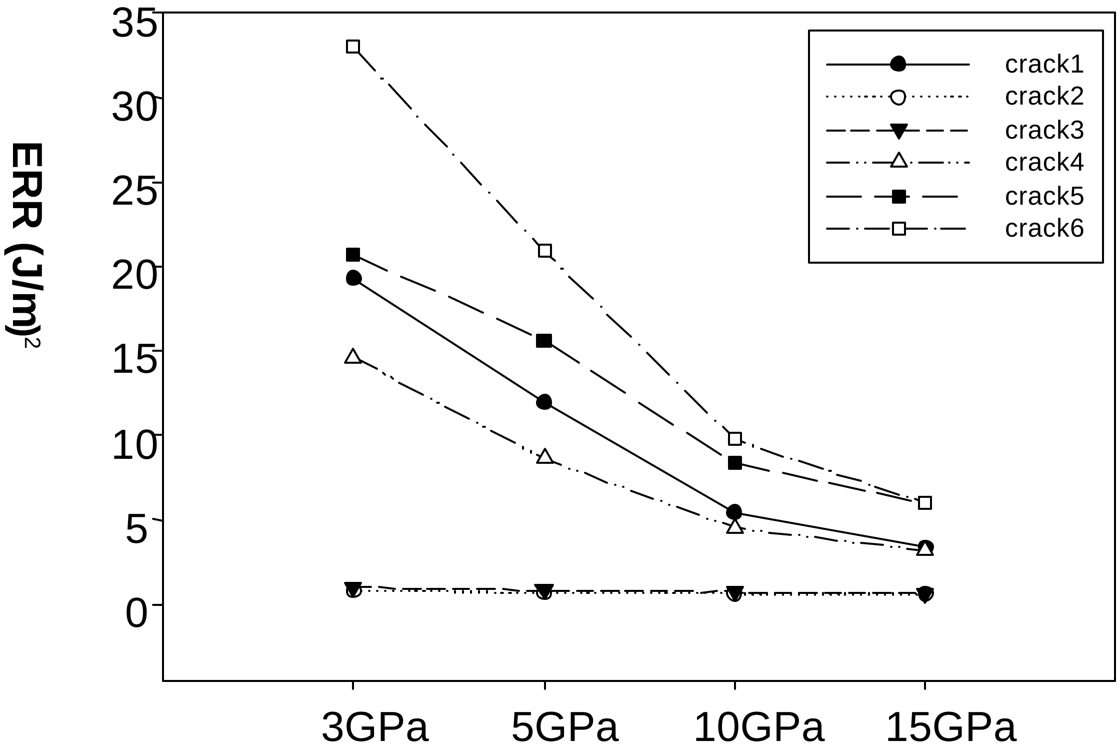
- Introduction of new materials*
- Integration of new processes and structures*
- Achieving necessary reliability
- Attaining dimensional control
- Manufacturability and defect management to meet overall cost/performance requirements

Five difficult challenges for <65nm beyond 2007

- Dimensional control and metrology
- Patterning, cleaning and filling high aspect ratio features
- Integration of new processes and structures
- Continued introductions of new materials and size effects
- Identify solution to address global scaling issues*

* Top three challenges

Effect of elastic modulus on ERR



ERR decreases with increasing elastic modulus of low k materials. The effect is almost linear. Uchibori et al., IITC 2006